On the Integration of Wide Band-gap Semiconductors in Single Phase Boost PFC Converters

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Ph.D. Dissertation, November 2015

DTU Electrical Engineering
Department of Electrical Engineering

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Preface and Acknowledgment

This thesis is submitted in partial fulfillment of the requirements for obtaining a PhD degree at Technical University of Denmark. The research has been carried out at the Electronics group in the Elektro Department from December 2012 to November 2015 under the supervision of prof. Michael A.E. Andersen and senior researcher Lars. P. Petersen.

The PhD project "Single Phase PFC using Wide Band-gap Devices" is part of Intelligent Efficient Power Electronics (IEPE) which is founded by Innovation Fund Denmark and The Obel Family Foundation with the following collaborating universities and companies:

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- Grundfos Holding A/S
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- KK Wind Solutions
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Abstract

Power semiconductor technology has dominated the evolution of switched mode power supplies (SMPS). Advances in silicon (Si) technology, as the introduction of metal oxide field effect transistor (MOSFET), isolated gate bipolar transistors (IGBT), superjunction vertical structures and Schottky diodes, or the introduction of silicon carbide (SiC) diodes, provided large steps in miniaturization and efficiency improvement of switched mode power converters.

Gallium nitride (GaN) and SiC semiconductor devices have already been around for some years. The first one proliferated due to the necessity of high frequency operation in optoelectronics applications. On the other hand, Schottky SiC power diodes were introduced in 2001 as an alternative to eliminate reverse recovery issues in Si rectifiers. Wide band-gap semiconductors offer an increased electrical field strength and electron mobility compared to Si semiconductors. Moreover, both semiconductor materials are particularly interesting for high temperature operation. These characteristics makes integration of SiC and GaN devices as the next logical step to further increase efficiency and power density in SMPS.

This work is part of the PhD project "Single phase PFC converter using wide band-gap devices" and focuses on attainable advantages by introducing wide band-gap semiconductors, and more particularly GaN devices in power factor correction circuits (PFC).

First, an overview of current state-of-the-art semiconductor technology in the 600/650 V range, and recent developments on the integration of GaN devices in SMPS are provided. The second part of the thesis provides an insight on semiconductor characterization and compares state-of-the-art Si technology to current available GaN switches. After this overview, a comparison between continuous (CCM) and boundary conduction modes (BCM) in PFC applications is provided based on the semiconductor characterization data. The comparison takes into consideration the electro magnetic interference (EMI) filter size and the converter input inductor volume, as a necessary part for evaluating the converter efficiency and power density. The last part of the thesis provides technical aspects on the controllability of GaN switches in high switching frequency implementations. Moreover, a zero voltage switching (ZVS) control scheme for BCM implementations, capable of operating in the MHz switching frequency range is presented.

Dansk Resumé

Effekthalvleder teknologien har domineret udviklingen indenfor højfrekvens omformere (SMPS). Fremskridt indenfor silicium (Si) teknologien som introduktionen af MOSFETs, IGBTs, superjunction vertikale strukturer og Schottky dioder samt siliciumkarbid (SiC) dioder, har gjort det muligt at gøre store fremskridt indenfor effekttæthed og øget effektivitet af SMPS.

Galliumnitrid (GaN) og Siliciumkarbid (SiC) halvlederkomponenter har været tilgængelige i noget tid. Disse teknologier blev i første omgang drevet frem af nødvendigheden for højfrekvensdrift i opto-elektroniske applikationer. SiC blev også introduceret i 2001 som et alternativ til standard silicium dioder med den klare fordel ikke at have reverse recovery effekter.

Halvledere med højt bånd gabs spænding kan håndtere en øget elektrisk feltstyrke og har en større mobilitet af elektroner i forhold til Si halvledere. Desuden er begge halvledermaterialer, GaN og SiC, særligt interessante da de ligeledes fungerer i højere drift temperaturer i forhold til Si. Disse egenskaber gør integrationen af SiC- og GaN-baseret halvledere endnu mere attraktive og det næste logiske skridt for yderligere at øge effektiviteten og effekttæthed i SMPS.

Dette arbejde er en del af ph.d.-projektet "Single phase PFC converter using wide bBand-gap devices" og fokuserer på opnåelige fordele ved at indføre halvledere med højt bånd gabs spænding og især GaN transistorer til strømforsyninger med effekt faktor korrektion (PFC).

Den første del af afhandlingen er et overblik over aktuelle state-of-the-art halvleder teknologier i spændingsklassen 600/650 V, og den seneste udvikling indenfor udbredelsen af GaN transistorer i SMPS. Efterfølgende del af afhandlingen giver et indblik i halvleder karakterisering og sammenligner state-of-the-art Si teknologier med nuværende tilgængelige GaN transistorer. Næste afsnit omhandler en sammenligning mellem kontinuerlig strøm konvertering (CCM) og grænse strøm konvertering (BCM) i PFC-applikationer, baseret på den tidligere udførte halvleder karakterisering. Sammenligningen tager hensyn til filter størrelse og spole volumen til filtrering af Elektro Magnetisk Interferens (EMI) som en nødvendig del for at vurdere, konverterens effektivitet og effekttæthed. Den sidste del af afhandlingen giver tekniske aspekter vedrørende styringen af GaN transistoren ved høj skiftefrekven. Desuden beskrives en metode til at tænde/slukke transistoren ved nul spænding (ZVS) når konverteren anvender BCM kontrol op i MHz området.

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Introduction

1.1 Background and Motivation

The proliferation of domestic and industrial appliances where the utilization of conventional ac/dc bridge rectifier circuits lead to load currents with high harmonic distortion, derived in the creation of the international IEC61000-3-2 [1] and European standard EN61000-3-2 [2]. These standards set a limit to the harmonic current distortion in equipment connected to the grid. Active power factor correction circuits were introduced to reduce harmonic distortion and comply with the limits set by the standards. Active power factor correction (PFC) circuits are based in switched-mode power converters where reactive elements are combined with semiconductor switches to control voltage and current. The reactive components act as energy storage elements, and their size is determined by the converter switching frequency. Increasing the converter switching frequency leads to reduced volume, weight and cost of the converter. However, the semiconductor switches present switching losses that put a practical limit on the maximum attainable switching frequency.

Since the introduction of the first power semiconductors in 1952 [3], Silicon (Si) has been and remains the main semiconductor material in switched-mode power conversion applications. However, wide band-gap semiconductor materials have been considered to be the next logical step since the mid 20th century [4]. It was not until 2001 that the first Silicon Carbide (SiC) wide band-gap power semiconductor was commercially available. Nowadays, gallium nitride (GaN) wide band-gap semiconductor material is also available. This semiconductor material that was previously used in light emitting diode applications, has arrived as a serious replacement for Si technology in power conversion applications. SiC and GaN market growth [5] reflects the superior characteristics of these semiconductor materials respect to Si with lower conduction and switching loss and higher temperature operation.

Integration of wide band-gap semiconductors as a replacement for Si technology in active PFC applications, which represent a growing market who reached 2.2 billion units world wide in 2011 [6], can provide efficiency and power density improvements, which have a large repercussion in energy and cost savings respectively.

1.2 Project Objectives

This project is based on the study of attainable advantages by substituting Si with wide band-gap semiconductors in single phase PFC applications. The main project objective was to study the main differences compared to current Si technology when integrating wide band-gap semiconductors in conventional PFC applications. In particular:

- To compare semiconductor loss based on characterization data and identify the strength of the different available semiconductor technologies.
- Study the impact of semiconductor technology on converter efficiency and power density.
- Investigate and identify the challenges on controllability due to the integration of the new semiconductor technology.

1.3 Thesis Scope

The scope of this PhD thesis is to summarize and present a coherent overview of the work carried out by the author as part of the PhD project "Single phase PFC using wide band-gap devices" from December 2012 until November 2015. This thesis presents key aspects on the integration of gallium nitride (GaN) switches as a replacement for existing silicon (Si) technology in power factor correction (PFC) applications with special focus on high efficiency, and high switching frequency operation.

The obtained results during this research period has been published in the form of peer reviewed conference and journal papers, as well as a pending patent application. These represent an important part of this PhD thesis and have been included in an Appendix at the end of this document.

1.4 Thesis Structure

Figure 1.1 shows the thesis structure, which consists of seven chapters. Following the introduction, chapter two provides an overview of current state-of-the-art semiconductor technology. The third chapter provides an inside into semiconductor characterization and compares vertical super junction structures to GaN cascode switches. Following, the fourth chapter of this thesis presents an evaluation of the characterized semiconductors in conventional boost PFC circuits operating in continuous (CCM), discontinuous (DCM), and boundary (BCM) or critical conduction mode (CrM). This evaluation takes aspects as the input conducted electromagnetic interference (EMI) filter and inductor size into consideration. Chapter five provides an overview on the controllability of GaN switches in high frequency implementations with special focus on BCM operation. Additionally, a new adaptive zero voltage switching (ZVS) control method for BCM implementations is proposed. Chapter six presents the conclusion obtained from this thesis together with a discussion on future work. Finally, other research topics are presented in chapter seven.

1.4 Thesis Structure

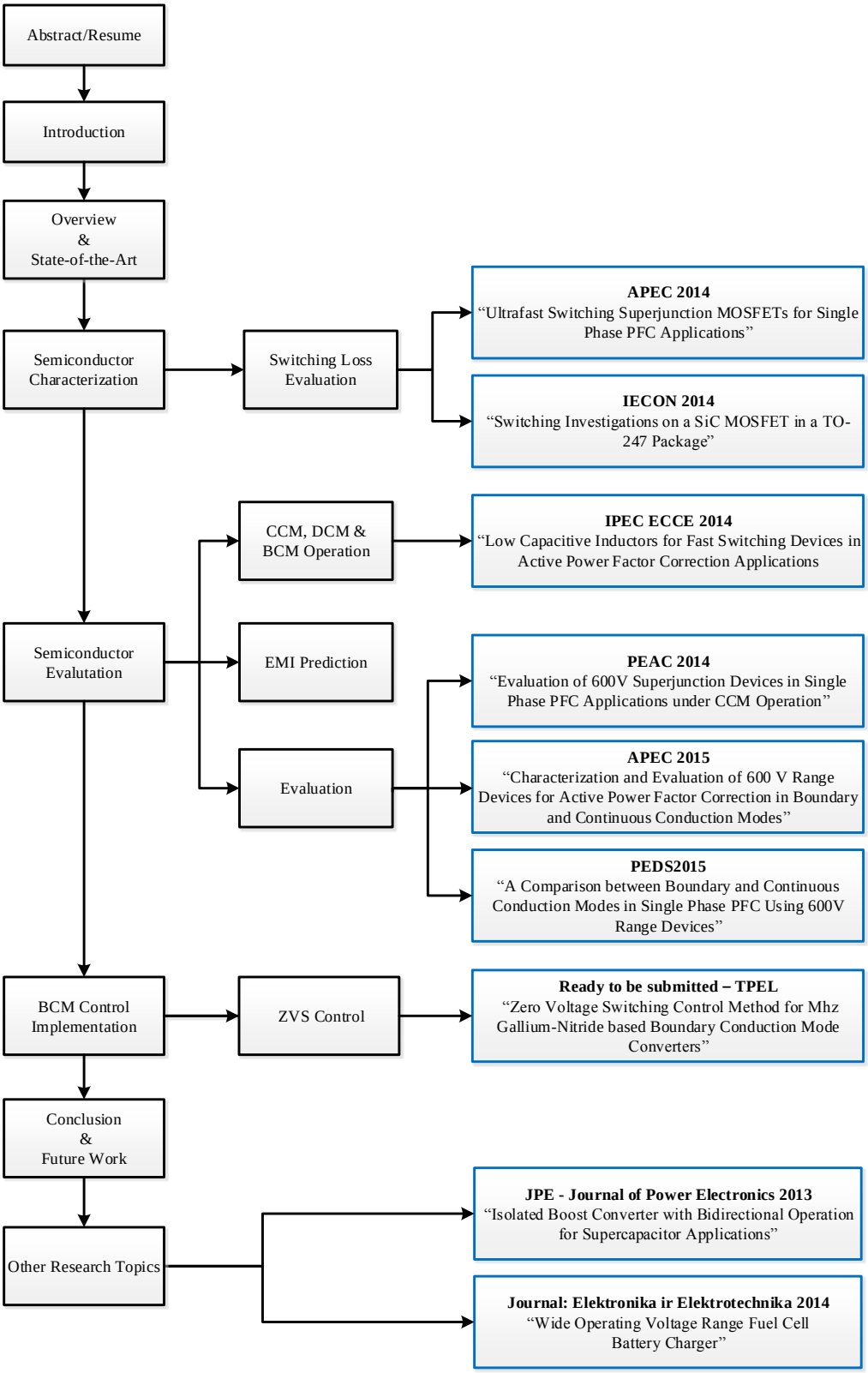


Figure 1.1: Thesis structure.

2

Overview and State-of-the-Art

2.1 Power Factor Definition

Simple alternating ac current circuits have sinusoidal voltage and current waveforms. When the load in this type of circuit is purely resistive, voltage and current waveforms are in phase and all the power delivered to the load is real P. When reactive components are inserted into the circuit, the complex impedance creates a phase difference between the voltage and the current creating a reactive power flow Q. The complex power resulting from the combination of real and reactive power flows is known as apparent power $S = P + jQ$.

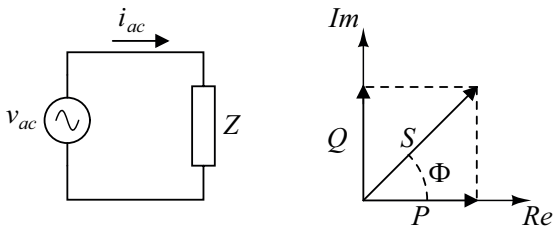
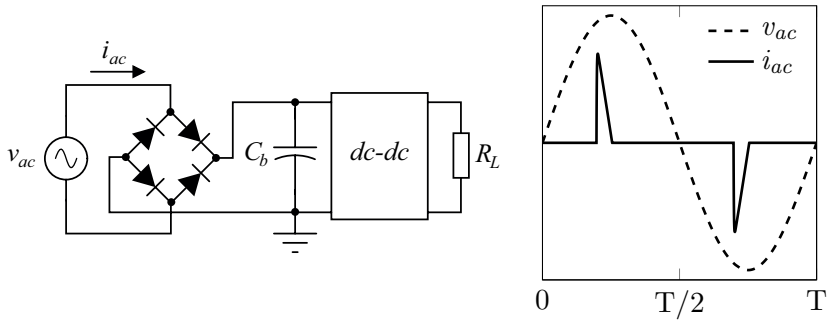


Figure 2.1: Simple ac circuit and complex power vector composition.

Power factor PF is the ratio between real P and apparent power S at any point in the power distribution grid. When linear loads are applied to the grid, the PF can be defined as in (2.1)

$$PF = \frac{P}{S} = cos(\Phi) \tag{2.1}$$

When the grid is loaded with reactive loads, the phase angle between voltage and current deviates from zero decreasing the power factor. Under this situation, the reactive current increases the grid losses for the same amount of real power delivered to the load. From the electricity provider point of view, a low power factor means that they have to provide a higher power than the real power consumed by the end user, and they have to deal with higher transmission and distribution losses. Therefore, a low power



(a) **(b)**

Figure 2.2: Conventional bridge rectifier configuration (a) and voltage and current waveform (b).

factor will be penalized in the electricity bill. Most of the reactive loading present in the grid is caused by industrial motor inductive loads. This type of reactive loading is commonly compensated by switched capacitor banks that increase the power factor locally, avoiding increased distribution losses and electricity bill penalties.
On the other hand, modern electronic appliances require from dc regulated voltages for operation which normally comprises of a ac to dc rectifier followed by a dc to dc power supply (Figure 2.2a) that adapts and regulates the dc voltage supply according to the appliance requirement. This type of load not only alters the Φ angle between voltage and current, but inserts a high content of current harmonic distortion. This type of circuit rectifies the ac voltage and charges the dc link capacitor to the peak maximum voltage. During the interval where the grid voltage is smaller that the capacitor voltage, the diodes in the bridge rectifier are in blocking state, and the capacitor is supplying the current to the load. When the grid voltage reaches again the capacitor voltage level, the capacitor gets charged with a current shape that posses a high content of harmonics as shown in Figure 2.2b.

When non-linear loads are applied to the grid, assuming the grid voltage is not heavily distorted [7], the power factor can then be redefined as in (2.2).

$$PF = \frac{P}{S} = \frac{P}{V_{ac,1,rms} I_{ac,1,rms}} \cdot \frac{1}{\sqrt{1 + (THD/100)^2}} \tag{2.2}$$

Where P is the real part of the deliver powered and can be calculated as in (2.3)

$$P = \sum_{k=1}^{\infty} V_{ac,k,rms} I_{ac,k,rms} \cdot cos(\Phi_k) \tag{2.3}$$

And where the THD or current harmonic distortion can be calculated as the ratio between harmonics as in (2.4)

$$THD = \frac{\sqrt{\sum_{k=2}^{\infty} I_{ac,k,rms}^2}}{I_{ac,1,rms}} \cdot 100\% \tag{2.4}$$

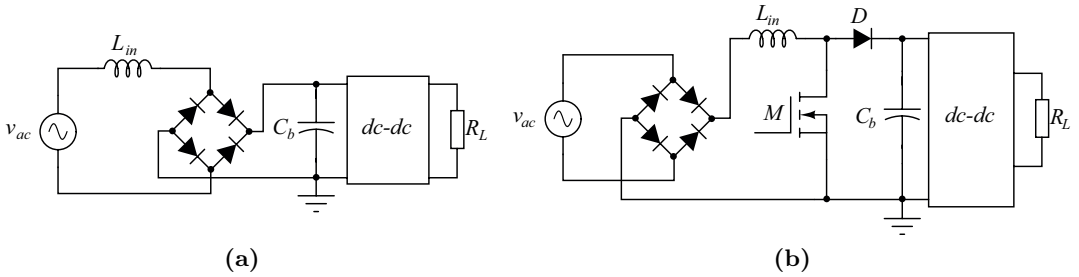


Figure 2.3: Passive (a) and conventional two stage active (b) PFC schematics.

In order to regulate the harmonics injected into the grid by all type of non-linear loads, a standard IEC/EN61000-3-2 dictates the harmonic current limits [1],[2] for different type of equipment with an input current smaller than 16 A per phase. The current limits are divided into some different classifications:

- Class A: Balanced 3 phase equipment, household appliances excluding equipment identified as class D, non portable tools, dimmers for incandescent lamps, audio equipment and all other equipment except the stated on the following classes
- Class B: Portable tools and non professional arc welding equipment
- Class C: Lighting equipment
- Class D: Pc, PC monitors, radio and television equipment with an input power $75\ W < P < 600\ W$

Class C and D equipment have limits relative to the power level, however classes A and B have absolute limits making possible for some of this applications to use the conventional bridge rectifier configuration without PFC compensation. For the rest of the classes some type of power factor correction is necessary. The most simple solution is the passive PFC (Figure 2.3a) that inserts an inductor in series with the bridge rectifier so the current harmonics are reduced; however, the inductor size makes this solution viable only at low power levels. Active PFC circuits are based on switched-mode converters where one or more than one active switch is used. The most adopted approach is the conventional two stage approach based on ac-dc power stage followed by a dc-dc converter as shown in Figure 2.3b.

2.2 Wide Band-gap Semiconductors

Switched-mode power supplies (SMPS) achieve voltage or current regulation by combining switches with energy storage elements. Compared to other solutions based in linear regulator circuits, SMPS can ideally achieve efficiencies $\eta = 100\ \%$. This type of technology was introduced early on the 20^{th} century, first using mechanical switches, vacuum tubes and finally semiconductor based switches [8], [9], [10], [11]. The reactive energy storage elements in SMPS are the largest and usually the most expensive components in these systems. The size of the storage elements is proportional to the energy storage requirement, which is determined by the converter power requirement and operating switching frequency. Therefore, increasing the converter operating frequency

Table 2.1: Wide Bandgap vs. Silicon Properties.

Properties	Si	4H-SiC	GaN
Bandgap E_G $[eV]$	1.12	3.26	3.39
Critical Field E_{crit} $[MV/cm]$	0.23	2.2	3.3
Thermal Conductivity λ $[W/cm \cdot K]$	1.5	3.8	1.3
Electron Mobility μ $[cm^2/V \cdot s]$	1500	650	2000
BFOM rel. Si	1	500	1300

allows to reduce the size of the energy storage elements which directly has an impact on the converter volume, power density and cost. However, the switches, far from being ideal, present switching losses due to overlapping between voltage and current during the switching transition. These losses put a practical limit on the converter operating frequency. Resonant topologies have been throughly investigated in the literature where extra reactive elements are inserted in order to eliminate the voltage-current overlap at the switching transition [9] allowing for an increased switching frequency. However, resonant topologies get penalized in conduction losses due to the reactive energy circulation in the circuit. Therefore, semiconductor technology, has been always the main driver in the evolution of SMPS towards higher efficiency and power density designs [12].

Silicon (Si) semiconductor material has been and remain the most used material in power electronics applications. The maturity of Si semiconductors and the optimization of the fabrication processes, has placed Si derived technology close to the theoretical material limits, leaving small room for further optimization [4]. As presented in Table 2.1, wide band-gap materials posses larger electrical field strength than Si, which makes possible to achieve lower specific on resistances due to the reduction in the channel length and consequently achieve a lower Baliga's Figure of Merit (BFOM) [13], [14], [15]. The reduction in the specific on resistance allows for a reduced die size for the same on resistance, which together with a decreased dielectric permittivity ϵ compared to Si, results in decreased parasitic capacitances which are responsible for the device switching speed limitation. Gallium nitride (GaN) and silicon carbide (SiC) are the main semiconductor materials adopted in the production of power semiconductors. The lower intrinsic carrier concentration in both materials compared to Si, reduces the leakage currents making possible to increase the semiconductor operating temperature. Moreover, the thermal conductivity of SiC and the stable on resistance r_{DS-on} in GaN devices, makes this materials ideal for high temperature and high power density converter implementations.

The main disadvantage of wide band-gap semiconductors is the increased price compared to Si (0.1 €/cm^2). SiC processes allow wafer implementations up to 6 inches with 10 €/cm^2 price, although 6 inches wafer capabilities have already been demonstrated [16]. On the other hand bulk GaN is an expensive material (100 €/cm^2), however epitaxial grow of GaN on Si substrate, has made this material to become an interesting solution in low and medium voltage range. Epitaxial grow on Si reduces the substrate price and allows for implementation of the current Si fabrication processes. Eight inches GaN on Si wafers have already been demonstrated. Moreover, if GaN on Si substrate is used, the price of a GaN based semiconductor could be theoretically lower than that of the Si alternative for the same current level according to BFOM

presented in Table 2.1. A forecast predicts GaN will replace Si metal oxide effect transistors (MOSFET) for voltages lower than 600 V and SiC will replace current isolated bipolar junction transistors (IGBT) for higher voltage ranges [17].

2.3 Active Power Factor Correction Circuits

Several approaches to achieve power factor correction, as presented in [18], have been investigated in the literature and can be divided into two main groups; those who achieve sinusoidal input current emulating a purely resistive load, and those who present high current distortion and are often limited to low power levels to comply with the standard. Inside these groups we can find two different approaches. The first approach, is the conventional two stage system presented in Figure 2.3b where a first stage operates as power factor corrector pre-regulator, and a second stage adapts the dc-dc level. The second approach includes all the single stage systems [19], [20], [21], [22], where the main goals are a reduction in the complexity, or an increment of the system efficiency by reducing the number of times the power is processed. However, these configurations are not as flexible as the traditional two stage solution, and often the increased current or voltage stress penalizes the overall system efficiency [23].

When sinusoidal input current and universal mains voltage operation are required, the conventional two stage approach is the preferred solution. In this type of implementation, the preferred topology for implementing the PFC pre-gulator is the boost topology due to its simplicity and ability to operate under universal input mains [18]. Several improvements have been proposed in the literature regarding this solution that can be summarized in two groups. The first one is to remove the bridge rectifier circuit to reduce the semiconductor conduction loss, and the second one is to include resonant or quasi resonant switching operation to reduce semiconductor switching loss [24]. Bridgeless topologies [25], [26], [27], [28], [29], [30] provide a significant efficiency improvement compared to conventional topologies, however, they present common mode noise issues [31] which limit their application. Resonant or quasi resonant topologies often include auxiliary circuitry [32], [30] to achieve zero voltage (ZVS) or zero current switching (ZVS) operation, or modify the switch operation to achieve these conditions operating in the boundary of continuous (CCM) and discontinuous conduction mode (DCM) [33]. These solutions reduce the semiconductor switching losses allowing for an increased converter switching frequency. On the other hand, resonant designs present an increased conduction loss than the equivalent hard switched implementation, due to higher voltage or current stress caused by the reactive energy circulation in the circuit.

In order to increase the PFC pre-regulator stage power density and efficiency, several aspects need to be taken into account. In order to reduce the energy storage requirement, the converter switching frequency needs to be increased. However, increasing the converter operating frequency will only have an effect on the input inductor size. This is because the converter input current presents a large 100 Hz ripple component necessary to achieve unity power factor. Hence, the output capacitance value needs to be large enough to filter this low frequency ripple to an acceptable level, that will depend on the application output power. However, if a regulator circuit is inserted after the capacitor to minimize the voltage ripple, makes it is possible to reduce the capacitor size [34]. Although, this technique will increase the converter complexity and affect negatively the efficiency, even considering that the proposed solution only processes

part of the PFC pre-regulator output power.

Therefore, it can be said that increasing the PFC pre-regulator switching frequency will reduce the converter input inductor size. Nevertheless, there are two possible negative effects to the converter volume or power density. First, if the semiconductor switching loss is increased, the increased power dissipation will require a larger semiconductor heatsink. Moreover, this type of systems require an input filter in order to comply with the conducted electromagnetic interference (EMI) standards [35]. This standard specifies a limit to the system input current harmonics in the frequency range $0.15 - 30\ MHz$. Figure 2.4 shows the input filter corner frequency for a boost PFC CCM converter as a function of the converter switching frequency. As it can be observed, increasing the converter switching frequency increases the filter corner frequency, which reduces the input filter size [36], [37], [38]. However, three minima appear in the filter corner frequency at $50, 75$ and $150\ kHz$. This is due to the fact that selecting the converter switching frequency to be placed just below these frequency values will avoid getting the third, second, and first harmonic, respectively, of the converter switching frequency inside the specified measurement range. Therefore, in order to further reduce the size of all the components towards a high power density design, the switching frequency of the converter needs to be pushed well beyond the $150\ kHz$ limit ($350\ kHz$ in this case), and the selected semiconductor technology has to provide efficient power conversion under the specified operating conditions.

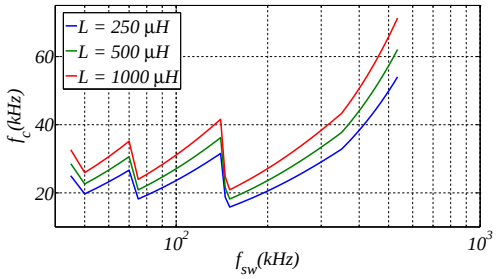


Figure 2.4: Input filter corner frequency vs. converter operating frequency for a CCM implementation at an output power level $P_o = 500\ W$.

2.4 State-of-the-Art

Semiconductor devices operating in conventional boost single phase PFC pre-regulators for universal mains belong to the 500-650 V operating range. In this operating voltage range, GaN and SiC devices outperform current Si semiconductor technology [39] in terms of specific on resistance. However, as it can be seen in Figure 2.5, current vertical superjunction Si structures have already surpassed the theoretical predicted Si limit [40], [41]. The advances in vertical superjunction structures, together with the room for optimization in the fabrication processes in wide band-gap semiconductors, makes the differences between Si and wide band-gap devices in this voltage range to be far from the predicted material ideal figures.

In hard switched converter applications, current GaN and SiC devices in the 500-650 V range do not offer a considerable improvement over state-of-the-art super junction

technology. This is because of the low capacitive switching energy loss in superjunction switches, which is equal or smaller than that of the equivalent GaN device [39], [42], [43]. This makes the improvement in terms of conduction and switching loss almost negligible. However, in resonant applications, the increased output capacitance charge (Q_{oss}) in superjunction penalizes the efficiency by increasing the root mean square (rms) current stress in the circuit, and consequently conduction losses. Moreover, as presented in [44], [45] vertical superjunction structures present a hysteresis loss during the charge and discharge of the parasitic output capacitance that is inversely proportional to the cell pitch and consequently inversely proportional to the on resistance. This makes state-of-the-art superjunction structures with low specific on-resistance non suitable for high frequency resonant implementations. Moreover, in applications that require use of the semiconductor body diode, superjunction vertical structures are penalized due to the large body diode reverse recovery loss [39], [46]. Therefore it can be said that the replacement of current Si technology in the 500-650 V range is application dependent.

Several vendors have released GaN High Electron Mobility Transistors (HEMT) in 600/650 V range. HEMT is a lateral device where a two dimensional electron gas (2DEG) is formed in the junction between a GaN and an aluminum gallium nitride AlGaN layer. This is a inherently a normally-on structure where several approaches have been adopted to produce a normally-off device [47]. The most adopted solution is the cascode configuration where a high-voltage normally-on HEMT is configured with a low-voltage Si MOSFET as shown in Figure 2.6.

When the cascode structure capacitances are properly balanced, the structure will present load current driven turn-off operation where the lower MOSFET parasitic output capacitance and the GaN HEMT input capacitance are charged in parallel by the load current [48], [49]. This property makes turn-off energy loss to be independent on the load current level, with a turn-off energy loss that corresponds to the stored energy in the device parasitic output capacitance. This characteristic makes GaN cascode devices to be a perfect candidate for CrM or BCM implementations, where valley switching or ZVS is achieved at the turn-on of the main switch, recovering part or the

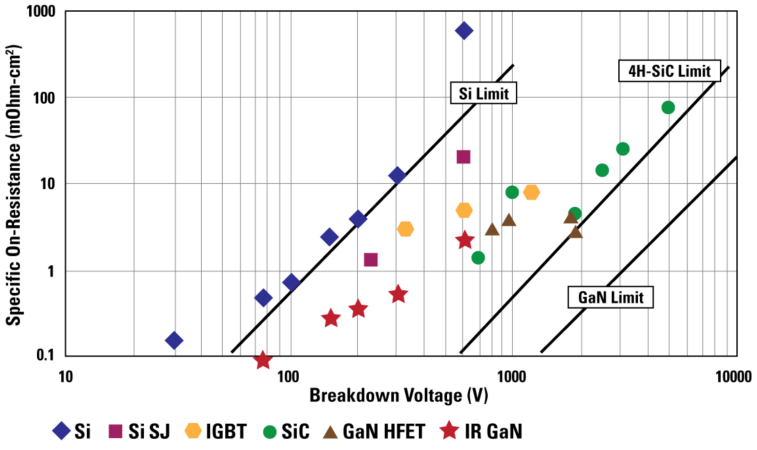


Figure 2.5: Si, SiC and Gan material specific on resistance theoretical limits for unipolar devices compared to state-of-the-art implementations.

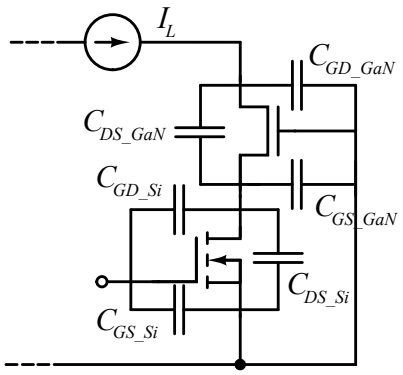


Figure 2.6: GaN-Si cascode structure with parasitic capacitances.

total energy stored in the device output capacitance during the turn-off process.

A comparative evaluation between superjunction and GaN HEMT switches is perfomed with GaN, Si and SiC diodes in several applications under hard switched conditions in [50]. A 1 MHz switching frequency isolated buck derived hard switched converter with efficiency $\eta = 87.2$ % is demonstrated in [51]. An evaluation of SiC diodes with superjunction Si switches in CCM PFC applications is presented in [52]. A comparison between Si and SiC diodes is presented in [53]. High switching frequency BCM GaN implementations have already been demonstrated in the literature where the increased current stress in BCM implementations respect to CCM operation gets compensated by the reduction in switching loss [54], [55]. A 5 MHz dc-dc BCM implementation with efficiency $\eta = 98$ % under ZVS conditions is demonstrated in [49]. A MHz GaN based BCM PFC converter is demonstrated in [56] with a peak efficiency equal to $\eta = 97.9$ %.

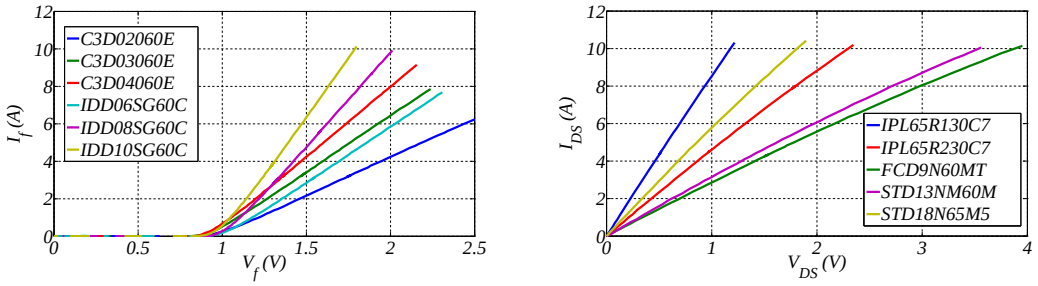
3

Semiconductor Characterization

Evaluation of the available semiconductor devices for the specific desired application through conduction and switching loss models is a powerful tool in the design of optimized switched-mode converters. This type of evaluation allows the designer to study a wide range of semiconductor devices under different operating conditions to find the most suitable technology for the required optimization objectives. There exist different ways to obtain a characterization model of the evaluated devices. The first and most accurate model is obtained from mixed-mode simulation models that include 2D finite element simulation models of the semiconductor structure linked to a circuit simulation program [45]. However, these type of simulations require large amounts of computational power and are not suitable for evaluating large number of semiconductors under a wide range of converter operating conditions. Another proposed solution is to derive a mathematical model of the evaluated semiconductor based on measured semiconductor output characteristics and parasitic capacitances [57]. This is an arduous work, however these models predict very accurately the switching behavior of the characterized devices decreasing considerably the computational power requirement from mixed-mode simulation models. Several analytical models are proposed in the literature for different semiconductor devices. A superjunction structure analytical model is proposed in [58] and validated with mixed-mode simulations. The work presented in [59] proposes an analytical model for SiC switches. A cascode GaN HEMT analytical model is presented in [48]. However, in order to produce models that accurately represent the device switching behavior at high switching frequency operation, a detailed knowledge of the device package structure is necessary to include the parasitic inductance effects [60], [61]. The last option is to accurately measure the device switching energy losses under a wide range of operating conditions with the conventional clamped inductive load circuit [62],[63].

3.1 Semiconductor Conduction Loss

Semiconductor conduction loss has to be calculated from the device characteristic curves. In the case of three terminal voltage controlled channel devices as MOSFET, Junction Gate Field Effect Transistor (JFET), or HEMFET the conduction loss can be calculated as $P_{cond} = I_{rms}^2 R_{DSon}$, where the switch equivalent resistance $R_{DSon} = dV_{DS}/dI_{DS}$ has to be obtained from the device characteristic output curve. In



(a) **(b)**

Figure 3.1: Measured characteristic I-V curves for different SiC diodes (a) and characteristic output curves for different superjunction MOSFETS for $V_{GS} = 12\ V$ (b) @ $25°C$.

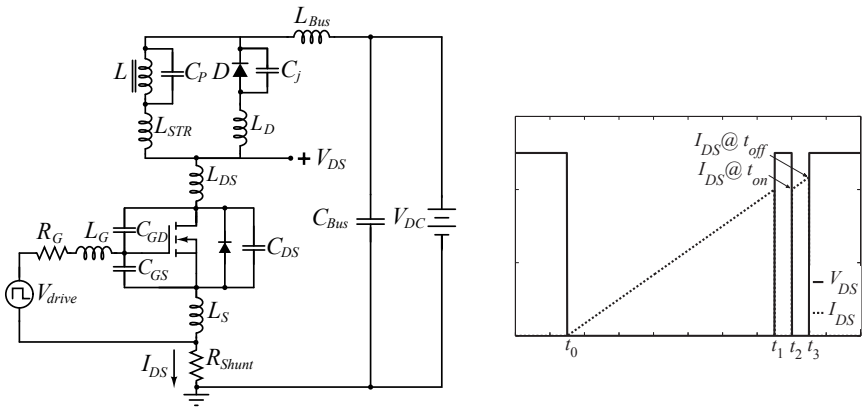
the case of devices with a forward biased junction as diodes, bipolar junction transistor (BJT), thyristors and insulated gate bipolar transistors (IGBT) $P_{cond} = I_{rms}^2 R_D + I_{av} V_t$, where V_t is the zero current forward voltage and the dynamic resistance can be calculated again from the I-V curve slope as $R_D = dV_f/dI_f$. The characteristic semiconductor curves can be obtained as a function of temperature by using a a semiconductor curve tracer [59], [64] or from the manufacturer datasheet. Figure 3.1a and Figure 3.1b show the characteristic I-V curves for different 600 V SiC diodes and for 600 V superjunction MOSFETs at room temperature.

This characterization procedure might not be sufficient for GaN HEMT devices, where a dynamic R_{DSon} phenomenon exist, as reported in [65]. This loss mechanism can be estimated by an oscilloscope measurement of the device voltage during on state using a clamp circuit as presented in [66]. However, most GaN manufacturers have reported this phenomenon not to be a significant issue anymore [47]. In this work, only static conduction loss is taken into account for GaN devices modeling. This phenomenon needs to be further investigated to study the influence of the dynamic R_{DSon} on the device conduction losses at high switching frequency operation.

3.2 Semiconductor Switching Loss

Switching loss can be evaluated using the traditional clamped inductive load test circuit shown in Figure 3.2a also known as double pulse tester (DPT). As can be seen in Figure 3.2b this circuit controls the inductor L current which is ramped up until the required characterization level is achieved at t_1. At this point, the main switch is turned off and the inductor current flows into the free-wheeling diode D. The main switch is turned on and off again, and the switching energy loss is obtained by integrating the voltage current product in the device in these switching events.

As the semiconductor switching speed capabilities increase, circuit and semiconductor package related parasitics become more critical in achieving the devices real potential [67], [59], [68], [69]. In this work, a four layer printed circuit board (PCB) design is used for implementing the DPT prototype (Figure 3.3a). The PCB is designed to minimize the area in critical current loops and to reduce parasitic inductance effects. The designed board is capable of accommodating surface mounted discrete packaging

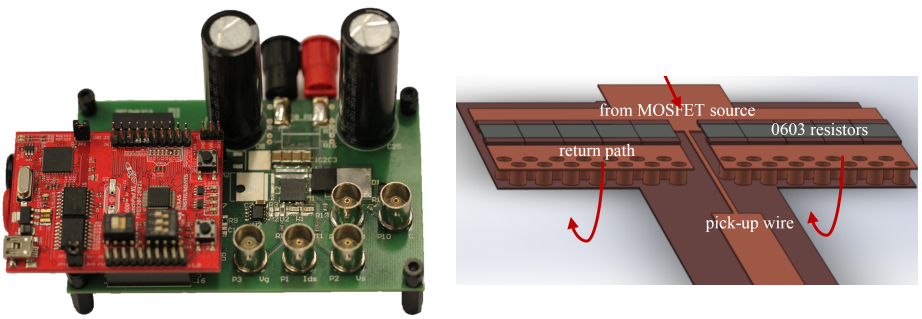


(a) **(b)**

Figure 3.2: Clamped inductive load test circuit or DPT schematic (a) and typical operating waveforms (b).

(DPAK) and power quad flat no-lead (PQFN) packages with kelvin connection for the gate drive source to reduce common source inductance effects [70]. A low parasitic capacitance inductor is implemented to reduce the contribution of this parasitic to the measured semiconductor capacitive switching loss [59], [63]. Another critical aspect in the implementation of the DPT prototype is the current measurement method. An overview on integration of current measurement techniques is presented in [71]. Current shunt resistors allow dc capabilities and easy implementation, however present bandwidth limitation and inaccuracy issues due to inductive coupling in the measurement loop and skin effect in the resistive element. A coaxial shunt structure is presented in [72], [73] that minimizes the inductive coupling in the measurement loop. These coaxial shunt resistors are commercially available nowadays with bandwidth specifications up to 2 GHz [74]. However, these devices presents a large insertion parasitic inductance $L = 2.2\ nH$ [59]. A low intrusive flat current shunt structure is proposed in [75], where the inductive coupling in the measurement loop is reduced by strategically placing the measurement voltage pick up wire in a low field intensity region. This structure is implemented with surface mount devices (SMD) thin film resistors to minimize skin effect issues. The structure shown in Figure 3.3b has been previously used in DPT circuits [62], [76].

Appendix A presents the implemented double pulse tester prototype and verifies the



(a) **(b)**

Figure 3.3: Implemented DPT prototype (a) and detail of the flat current shunt structure (b).

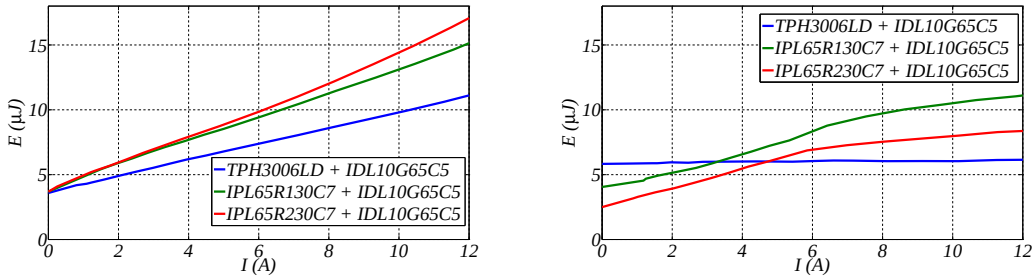


Figure 3.4: Measured switching energy loss for 600 V superjunction devices and cascode GaN HEMT. Turn-on (a) and turn-off (b) vs. current level.

current shunt transfer function with a finite element analysis (FEA) simulation. A comparison of state-of-the-art Si superjunction devices selected by their gate charge and on resistance ratio is performed. The superjunction devices are characterized with SiC diodes, and the switching losses are obtained for different gate resistors values and as a function of the temperature. The results from this characterization show the reduced switching loss attained by the latest released superjunction devices compared to older series.

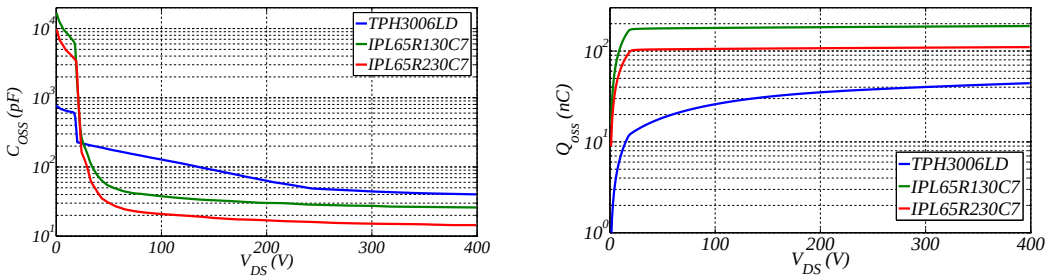
The best performing switches from the characterization presented in Appendix A are selected as a reference for comparison with GaN semiconductor devices during the duration of this project. Figure 3.4a and Figure 3.4b show the measured switching loss energy for two superjunction MOSFET devices with an on resistance of $R_{DS} = 130\ m\Omega$ and $R_{DS} = 230\ m\Omega$, and a cascode GaN HEMT with $R_{DS} = 150\ m\Omega$ in combination with a 10 A SiC diode. As it can be seen, the GaN switch presents slightly lower turn-on loss than the two superjunction switches. However, the turn-off measurement at zero current condition, which corresponds to the stored energy in the devices output capacitance, shows a lower capacitive loss for the superjunction structures. On the other hand, as the current level is increased, it can be observed that the cascode structure energy loss remains flat due to the load current driven turn-off mechanism elucidated in [48], [49]. This turn-off mechanism ensures very low channel energy loss, which makes cascode GaN a good candidate for BCM implementations where the increased turn-off current level will not have a negative effect on semiconductor switching loss.

3.3 Parasitic Capacitance

In order to evaluate the performance of the semiconductors in resonant applications, the parasitic output capacitance needs to be obtained. This can be done by using the setup shown in [77] or from the manufacturer datasheet. Figure 3.5a shows the parasitic output capacitance of the previously presented superjunction MOSFETs and cascode GaN HEMT switch. These non-linear capacitance values need to be used in order to calculate the resonant converter waveforms, and estimate capacitive switching loss under valley switching conditions as in [78]. Figure 3.5b presents the calculated output capacitance charge vs. V_{DS} voltage. As it can be observed, the two super-

junction structures that presented lower capacitive energy loss in Figure 3.4b posses a much larger capacitive charge than the GaN switch, which will increase the reactive current circulation in resonant applications increasing conduction losses and penalizing the system efficiency [39].

The joule loss associated to the charge and discharge of the parasitic output capacitance of the evaluated switches needs to be obtained to accurately predict the semiconductor losses under resonant operation. An equivalent series resistance can be obtained by using the setup presented in Appendix F. However, as shown in [45], depending on the semiconductor structure, different loss mechanisms can appear during the charge and discharge of the devices capacitance under resonant operation. The work presented in [44] shows a experimental setup to measure this capacitive joule loss in resonant circuits. These loss mechanisms needs to be further investigated in order to obtain more accurate semiconductor loss models. In this work, in order to simplify the models, the channel on resistance R_{DS} is used as the equivalent series resistance of the device output capacitance.



(a) **(b)**

Figure 3.5: 600 V superjunction devices and cacode GaN parasitic output capacitance C_{OSS} (a) and charge Q_{OSS} (b) vs. drain to source voltage V_{DS}.

4

Semiconductor Evaluation

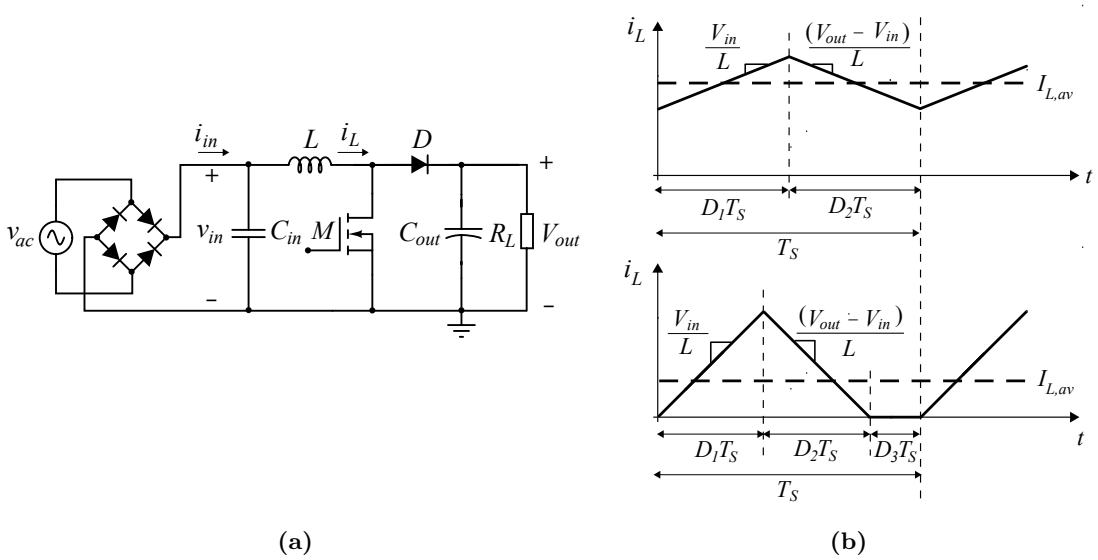
GaN cascode structures with a current driven turn-off mechanism are particularly interesting for BCM implementations [49], [54], [49]. Under this operation mode is possible to achieve valley switching or ZVS conditions recovering part or the total amount of energy stored in the switching node capacitance allowing for high switching frequency implementations. However, in order to evaluate the possible advantages that can be obtained from replacing Si devices with wide band-gap semiconductors, the evaluation needs to be performed from a system level point of view [37],[38],[36]. The evaluation procedure in this work is based on a comparison of semiconductor loss, input inductor, and filter size for a conventional boost PFC pre-regulator stage as shown in Figure 4.1a operating in BCM and CCM/DCM modes. In order to perform the evaluation, converter input inductor current shape is defined across half line cycle [79]. With the voltage and current shape defined across the line, the semiconductor loss can be calculated from the characterization data. Moreover, the energy storage requirement of the input inductor is calculated based on the peak current value, and the differential mode input filter corner frequency can be determined based on a conducted EMI prediction model.

4.1 CCM, DCM and BCM Operation

There exist three operation modes depending on the inductor current shape: CCM, DCM and BCM. The inductor current waveform of a boost converter under CCM/DCM conditions is depicted in Figure 4.1b. PFC CCM implementations require a dual control loop implementation [18] where a slow outer loop regulates the output capacitor voltage, and a fast inner loop regulates the input inductor current in order to achieve unity power factor. The converter inductor current will then operate under CCM/DCM conditions across the line cycle depending on the instantaneous conditions. The minimum instantaneous input converter current that determines the transition from CCM to DCM operation mode can be calculated by obtaining the inductor average current at the boundary between modes as shown in equation 4.1.

$$I_{in} = I_{L,av}\frac{M-1}{M} \cdot \frac{V_{in}T_s}{2L} \tag{4.1}$$

Where V_{in} is the instantaneous rectified input voltage and M is the converter input to output voltage ratio $M = V_{out}/V_{in}$. Once the boundary between modes is determined,



(a) **(b)**

Figure 4.1: Boost PFC circuit (a) and inductor current waveforms (b) CCM top and DCM bottom.

Table 4.1: Duty cycle derivation CCM/DCM.

Mode	CCM	DCM
D_1	$\frac{M-1}{M}$	$\sqrt{k \cdot M \cdot (M-1)}$
D_2	$1 - D_1$	$\frac{k \cdot M}{D_1}$
D_3	0	$1 - D_1 - D_2$

the current shape can be calculated by deriving the inductor current periods as shown in table 4.1.

It is also possible to implement a converter operating in pure DCM mode or in BCM mode. These type of implementations, also known as voltage follower [18], allow removing the inner current control loop maintaining a fixed switch on time D_1T_S across the line cycle to achieve unity power factor. Moreover, DCM and BCM implementations reduce the input inductor size, reduce the turn-on switching loss and mitigate the reverse recovery issues compared to CCM implementations [38]. On the other hand, DCM and BCM modes present a larger components current stress, which results in larger conduction losses and an increased converter input filter size.

BCM implementations operate at the boundary between CCM and DCM. The typical inductor current waveform of a BCM implementation is depicted in Figure 4.2. This operation mode presents a variable switching frequency across the line cycle that according to [80] can be calculated as shown in equation 4.2.

$$f_s(t) = \frac{1 - v_{in}(t)/V_{out}}{T_{on}} \tag{4.2}$$

Where T_{on} which remains constant during the line cycle corresponds to the switch

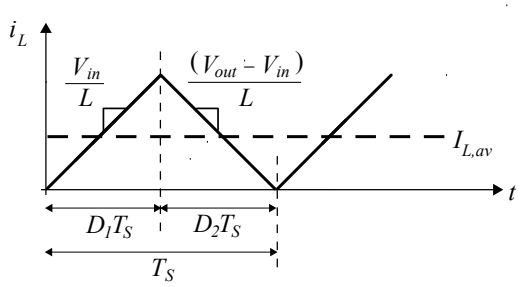


Figure 4.2: Ideal BCM current waveform.

conduction time $D_1 \cdot T_S$ and can be derived as in equation 4.3

$$T_{on} = \frac{2P_{in}L}{V_{ac,rms}} \tag{4.3}$$

However, practical BCM implementations include valley or ZVS switching by letting the input inductor resonate with the switch and diode parasitic capacitances (Figure 4.3). As can be seen in Figure 4.4, when the inductor reaches zero value and the diode becomes reverse biased, the capacitances attached to the converter switching node transfer part or the total amount of energy back the input inductor minimizing the switching loss. In order to accurately predict the converter switching frequency and inductor waveform, these resonant periods need to be accurately modeled with the semiconductor non-linear parasitic capacitances as presented in [81], Appendix E, Appendix F, Appendix G. Figure 4.5 shows the operating waveforms of a BCM implementation across half line cycle. As can be seen, the ideal switching frequency formula from eq. 4.2, fails to predict the converter switching frequency when a conventional PFC BCM controller with valley or ZVS switching is used. The major error in switching frequency prediction is caused by the negative inductor current during the valley switching that needs to be compensated by an increased switch on time, and consequently, a reduced switching frequency. Moreover, as it can be observed the converter switching frequency gets clamped close to the zero crossing of the ac input voltage. This effect occurs due to the intrinsic operation of constant on time controllers. As the converter input voltage is decreased, the fixed on time limits the input inductor current until the switching node voltage fails to reach the converter output voltage level. Under these conditions, no power transfer to the output occurs, and the diode bridge rectifier at the input makes the capacitor input voltage C_{in} to remain constant until the beginning of the next half line cycle.

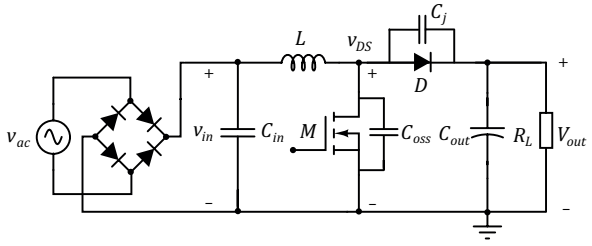


Figure 4.3: Conventional boost PFC pre-regulator with switching node parasitic capacitances.

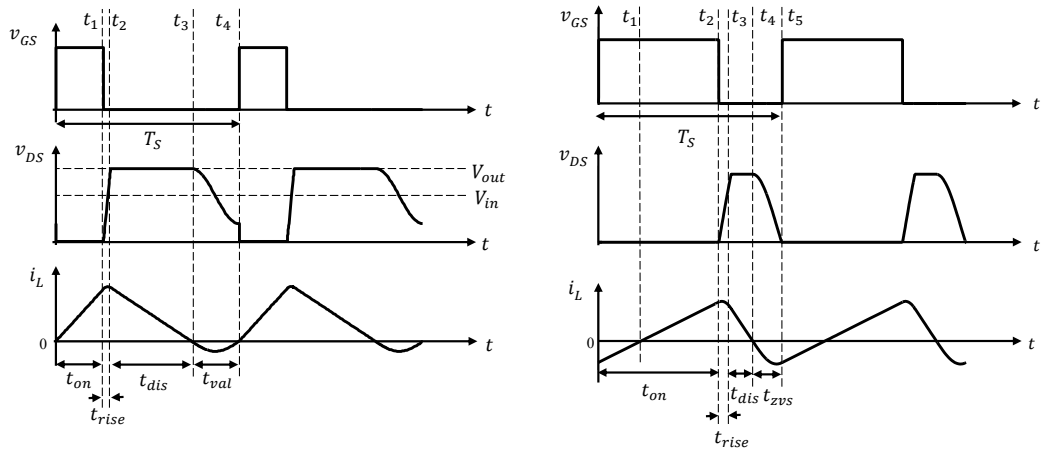


Figure 4.4: Characteristic operating waveforms under valley and ZVS conditions.

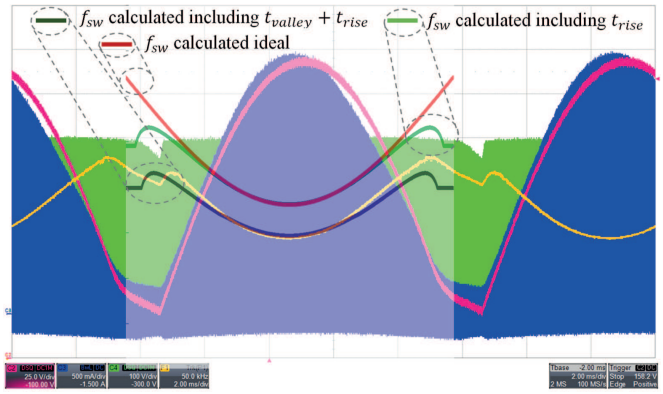


Figure 4.5: Measured vs. calculated PFC converter BCM switching frequency.

4.2 EMI Prediction

In order to calculate the input filter corner frequency that meets the required harmonic attenuation to fulfill the limits specified in the standards [35],[82],[83],[84],[85],[86] a conducted EMI prediction model is necessary . The characteristic setup for conducted EMI measurements is shown in Figure 4.6. The device under test (DUT) which in this case is the PFC pre-regulator stage, is connected to a line impedance stabilization network that normalizes the impedance seen from the DUT and acts as an interface to the electromagnetic compatibility (EMC) test receiver. A model for the EMC receiver and LISN network blocks depicted in Figure 4.7 is presented in [80], [87]. The differential conducted EMI spectrum can be calculated from the input inductor current definition for the three previously analyzed operation modes. Once the inductor current harmonics are calculated, the equivalent impedance of the LISN network used in the conducted EMI measurement setup, can be calculated as presented in Appendix D. From this equivalent impedance, it is possible to calculate the measured voltage V_A that is injected to the EMC receiver. The EMC receiver intermediate filter (IF) performs a sweep in the frequency range specified by the standard ($0.15 \leq f_i \leq 30\ MHz$ for CISPR22 [35] and CISPR14 [82]). The output of the IF filter is fed to an envelope detector, and the resulting envelope is inserted into the average and quasi peak detection circuits. Calculation of the quasi-peak value, involves a bisection or dichotomy

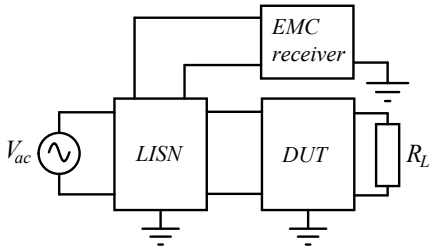


Figure 4.6: EMI measurement setup.

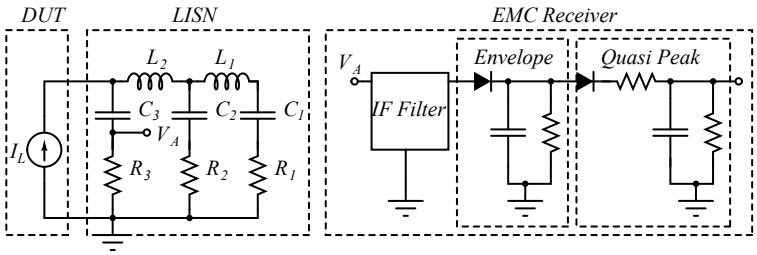


Figure 4.7: LISN network and EMI receiver block diagram.

method based on the quasi peak capacitor charge balance as presented in [80]. Once the quasi-peak and average values of the envelope signal are calculated as shown in Figure 4.8, the necessary filter attenuation and corner frequency can be predicted.

Figure 4.9a shows a measured vs. calculated conducted EMI voltage disturbance for a CCM implementation and Figure 4.9b shows the calculated vs. the measured inductor current average and quasi-peak values for a BCM boost PFC implementation for the operating conditions shown in Table 4.2. The BCM implementation measurement is performed in the inductor current in order to insert a decoupling capacitor at the input of the converter to provide a low impedance path to the high frequency inductor ripple content. As it can be observed, both calculations show good match with the calculated values. The BCM measurement, which is performed using a superjunction MOSFET IPL65R130C7 with a SiC diode IDL10SG65C5 and a FAN9612 BCM controller, shows a variable converter switching frequency in the range from $140 - 230\ kHz$ while the prediction shows $140 - 212\ kHz$. This deviation can be caused by the assumption that the converter switching frequency remains constant close to the input voltage zero

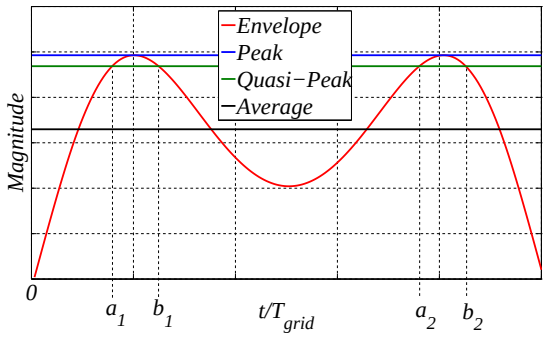
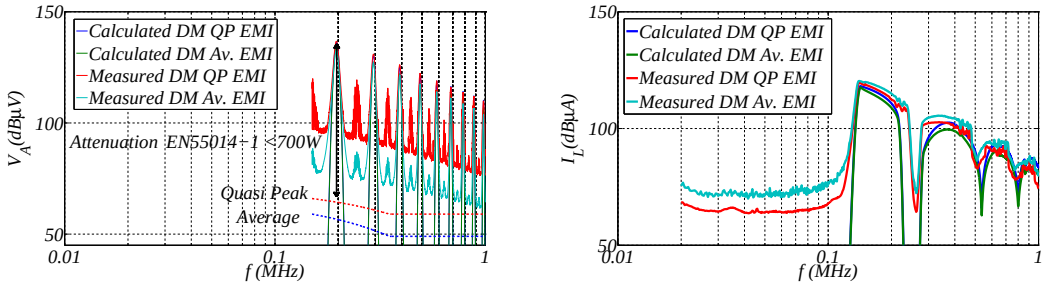


Figure 4.8: Envelope, average and quasi-peak waveforms.

Table 4.2: CCM and BCM converter operating conditions during conducted EMI measurement.

Mode	CCM	BCM
$V_{ac,rms}$	230 V	120 V
V_{out}	386 V	387 V
L	1150 μH	230 μH
P_{out}	200 W	100 W



(a) (b)

Figure 4.9: Measured vs. calculated EMI noise for a boost PFC operating in CCM (a) and BCM (b).

crossings as previously presented in section 4.1, when in reality, the converter losses contribute to the discharge of the converter input capacitor C_{in} slightly increasing the converter switching frequency.

4.3 Evaluation

A semiconductor evaluation is performed in this section by comparing estimated semiconductor performance based on characterization data, and attainable advantages in terms of input inductor and filter size reduction. This evaluation assumes that the size of these components is solely affected by the energy storage requirement of the input inductor and the corner frequency of the filter. However, the size of these components depends on many other parameters such as power dissipation, core material, core shape and winding structure. The work presented in [38] and [36] shows an optimization routine with focus on CCM and DCM operation modes, where a core database with two different winding structures are used. Even though this is the correct approach, considering all the possible variations between converter operating modes and operating frequency it is a tedious and challenging task that requires accurate magnetic component loss and thermal models for different winding and core structures. Therefore, the assumption of representing the inductor volume by its energy storage requirement does not provide an accurate representation of the component size, however, it provides a rough calculation for comparison between operating modes as a function of the converter switching frequency.

Appendix D shows an evaluation of inductor and filter size for superjunction and SiC devices operating in CCM with an input voltage $V_{ac} = 230\ V_{rms}$ and an output power

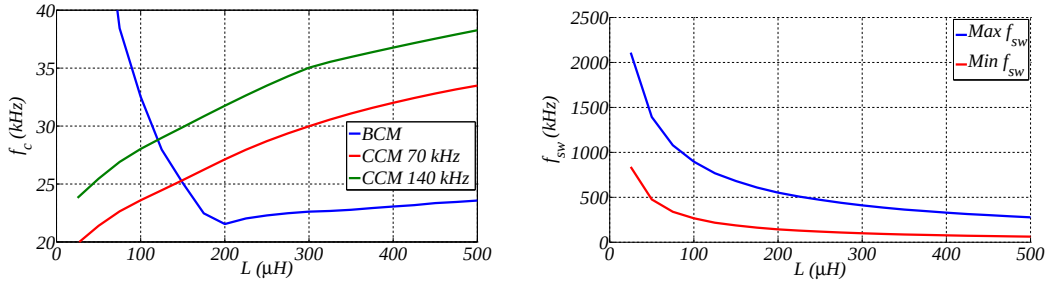


Figure 4.10: Calculated input filter corner frequency for a PFC boost converter operating in CCM and BCM modes as a function of the inductance value L (a) and calculated maximum and minimum switching frequency for a BCM implementation as a function of the inductance value L (b).

$P_{out} = 500\ W$. This analysis, shows a five times input inductor size reduction without penalties in the input filter corner frequency and with an increment of 3.15 $W\%$ in semiconductor loss at the evaluated power level. Appendix E presents a comparison between BCM and a CCM where semiconductor loss in two superjunction devices operating with a SiC diode is evaluated together with the energy storage requirement of the input inductor. Appendix F completes this work by including the EMI model in the comparison and evaluating the input filter corner frequency for both modes under $V_{ac} = 230\ V_{rms}$ and $P_{out} = 200\ W$. These evaluations show that a three times reduction in the input inductor energy storage requirement is possible for a 150 μH inductor BCM implementation without penalty in semiconductor loss compared to a 45 kHz CCM implementation at this power level.

Figure 4.10a shows the calculated input filter corner frequency for a cascode GaN based PFC operating at $V_{ac} = 230\ V_{rms}$ and $P_{out} = 200\ W$ in BCM, and CCM at $70kHz$ and $140kHz$ switching frequency. As previously presented in Section 2.3, the selected CCM switching frequencies correspond to the best case for the EMI input filter corner frequency. As it can be seen for the BCM case, it is possible to reduce the input filter size compared to the CCM implementation operating at 140 kHz, if the input inductor value is reduced under $L = 75\ \mu H$. Figure 4.10b shows the BCM operating frequency versus the inductor value. As it can be observed, selecting an input inductor value $L = 75\ \mu H$ will set a converter switching frequency range $f_{sw} = 0.35 - 1.1\ MHz$. It can be concluded that increasing the converter operating frequency towards the MHz operation range, as presented in [81], allows for a reduction of both the converter input filter and input inductor size under BCM operation.

Figure 4.11a shows a comparison between a 130 $m\Omega$ superjunction device and a 150 $m\Omega$ cascode GaN device with a SiC diode, evaluated for a CCM boost PFC at $P_{out} = 500\,W$. As it can be observed, the calculated semiconductor loss for the Si and the GaN device under these conditions are very close to each other. Moreover, as shown in Figure 4.11b where the same two devices are evaluated for a reduced power level $P_{out} = 50\ W$, it can be seen that the reduced capacitive switching loss of the superjunction structure results in a lower switching loss in the Si device compared to the GaN switch. It can be concluded that no real advantage is obtained by replacing the Si switches with cascode GaN in CCM applications. On the other hand, when the two devices are evaluated

in a BCM application as shown in Figure 4.12a, the large capacitance of the vertical superjunction structure at low voltage levels, increases the capacitive switching loss of the converter under valley switching operation. Consequently, as it can be seen in Figure 4.12b where the same devices are evaluated for an output power level $P_{out} = 50\ W$, the difference in efficiency loss due to capacitive energy loss is increased, making the advantage of the GaN over the Si device more clear. Additionally, as it can be seen in this figure, when the input inductor value is reduced under $L = 75\ \mu H$, the BCM implementation with the superjunction device is not able to regulate the output voltage of the converter anymore. This is due to the fact that, even if a zero on time is set by the controller that regulates the output voltage, the amount of current build in the converter input inductor during the charge of the device output capacitance, sets a lower limit on the amount of transferable energy per converter switching cycle.

It can be concluded that BCM PFC implementations allows for reducing the input inductor size compared to CCM implementations, but a reduction of the input filter size is only possible when the input inductor value is largely decreased moving the converter operating frequency into the MHz range. Moreover, as it was expected, replacement of superjunction Si devices with GaN cascode switches in CCM applications does not provide any efficiency gain, but the increased capacitive loss at low voltage levels of superjunction devices and the current driven turn-off mechanism of GaN cascode switches, makes these semiconductors the right choice for high frequency BCM implementations. Further experimental results need to be carried out to verify the proposed model. As presented in section 3.1, the dynamic R_{DSon} needs to be included to produce more accurate semiconductor models. Moreover, the joule loss during the charge and discharge of the switch output capacitance during resonant operation needs to be characterized and included in the model. A genetic algorithm as presented in [37], [38], [36], is necessary to produce a design tool to evaluate different designs for different optimization objectives.

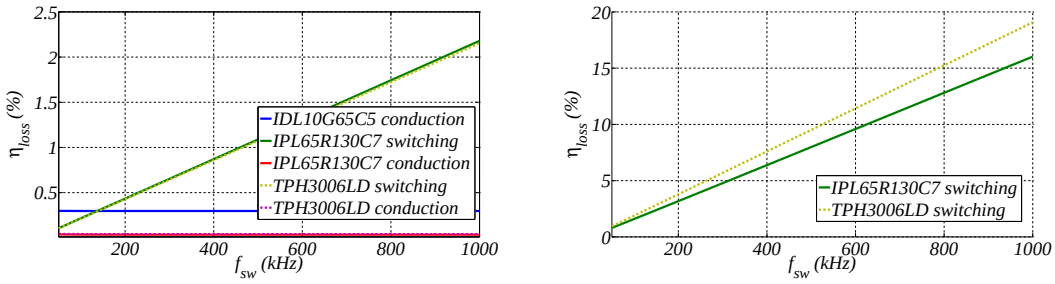


Figure 4.11: Calculated semiconductor loss as a percentage of the converter output power for a CCM implementation using a superjunction/SiC diode and a cascode GaN/SiC diode combination for $P_{out} = 500\ W$ (a) and $P_{out} = 50\ W$ (b).

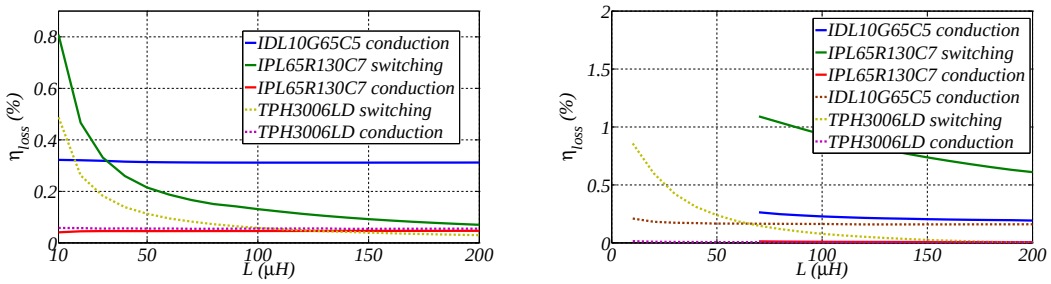
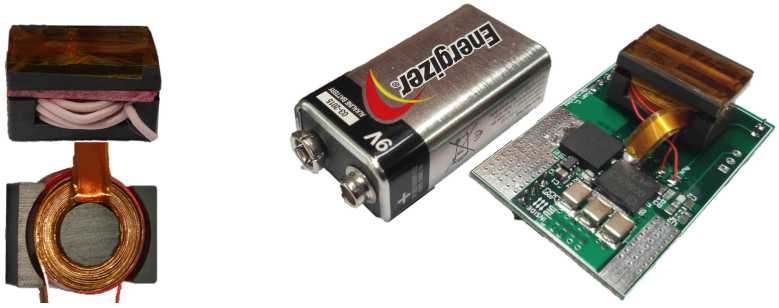


Figure 4.12: Calculated semiconductor loss as a percentage of the converter output power for a BCM implementation using a superjunction/SiC diode and a cascode GaN/SiC diode combination for $P_{out} = 500\ W$ (a) and $P_{out} = 50\ W$ (b).

4.4 BCM Power Stage Implementation

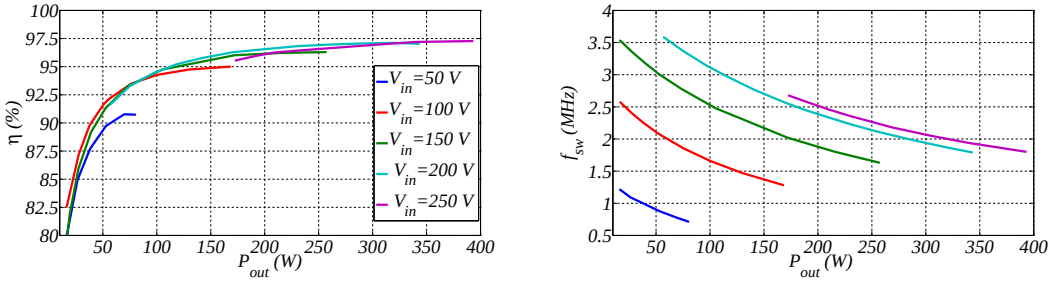
A boost power stage is implemented with the evaluated 150 $m\Omega$ cascode GaN device in a quiet tab package TPH3006LS and 10 A SiC diode IDL10G65C5. A four layer PCB design with 70 μm copper thickness is implemented, where the critical current loops and the PCB contribution to the switching node parasitic capacitance are minimized. A high current low propagation delay gate driver UCC27511 is used. The converter inductor is implemented using an EQ20R core with plate in 3F45 material from Ferroxcube. Figure 4.13a shows two implemented 11 μH 13 turns inductor prototypes with Litz 450/46 and 0.2 mm copper foil to analyze the trade-off between fill factor and proximity/skin effect. Figure 4.13b shows the implemented power stage. Figure4.14a and Figure 4.14b shows the measured efficiency and switching frequency for the power stage with the Litz wire inductor as a function of the converter output power P_{out}. Figure 4.15a and Figure 4.15b shows the same curves for the power stage with the foil inductor. The converter efficiency is measured under dc-dc conditions with 6 and 1/2 digit precision multimeters, and include the diode bridge rectifier conduction loss. As it can be observed, the implementation with the Litz wire inductor presents higher efficiency than the prototype with the foil winding inductor. This is due to the fact that the ac winding loss dominates over the low frequency component in MHz BCM implementations [89]. Even at low input voltage levels, where the converter switching frequency is decreased and the increased fill factor of the foil winding implementation should provide an advantage, the large amount of negative inductor current during ZVS operation increases the ac ripple component compared to the average value further penalizing the copper foil structure.

These efficiency measurements show the feasibility of achieving high efficiency in BCM MHz implementations; however, the converter inductor design needs to be further investigated analyzing different core shapes and Litz wire windings by using FEA simulations as presented in [89].



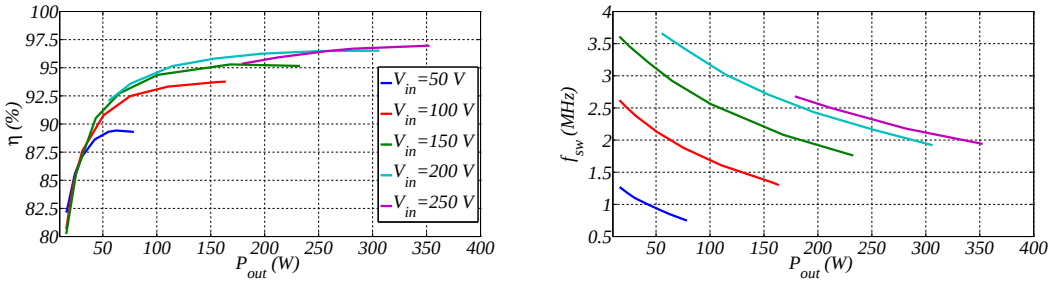
(a) (b)

Figure 4.13: Implemented EQ20R inductors (a) and conventional boost power stage (b).



(a) (b)

Figure 4.14: Measured power stage efficiency with Litz wire inductor including the bridge rectifier (a) and switching frequency f_{sw} (b) under dc input voltage conditions as a function on the converter output power P_{out}.



(a) (b)

Figure 4.15: Measured power stage efficiency with copper foil inductor including the bridge rectifier (a) and switching frequency f_{sw} (b) under dc input voltage conditions as a function on the converter output power P_{out}.

5

BCM Control Implementation

BCM operation of converters is based on a variable switching frequency control where the main switch gate signal is operated to regulate any state variable in the circuit while maintaining the input inductor current in the boundary between CCM and BCM as shown in Figure 5.1. These schemes need to detect or predict the inductor current zero crossing in order to determine the turn-on instant of the main switch. The most simple approach is to use current sense resistors to detect this condition, however, insertion of a resistive element in the current path produces conduction losses. Several approaches have been proposed in the literature to replace the current sense resistive element. Some solutions predict the zero crossing based on the converter operating voltages by using current mirrors to control the switch timings [90],[91],[92] and other implementations use digital signal processors to estimate the switch timing [93]. However, when BCM operation is implemented, valley switching or ZVS operation are preferred to reduce capacitive switching loss. This operation mode requires from a different control approach where the switching node voltage of the converter is sensed for determining the turn-on instant of the main switch in the converter.

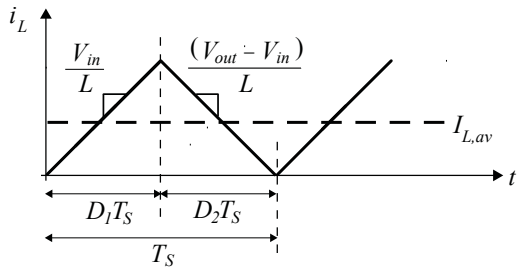
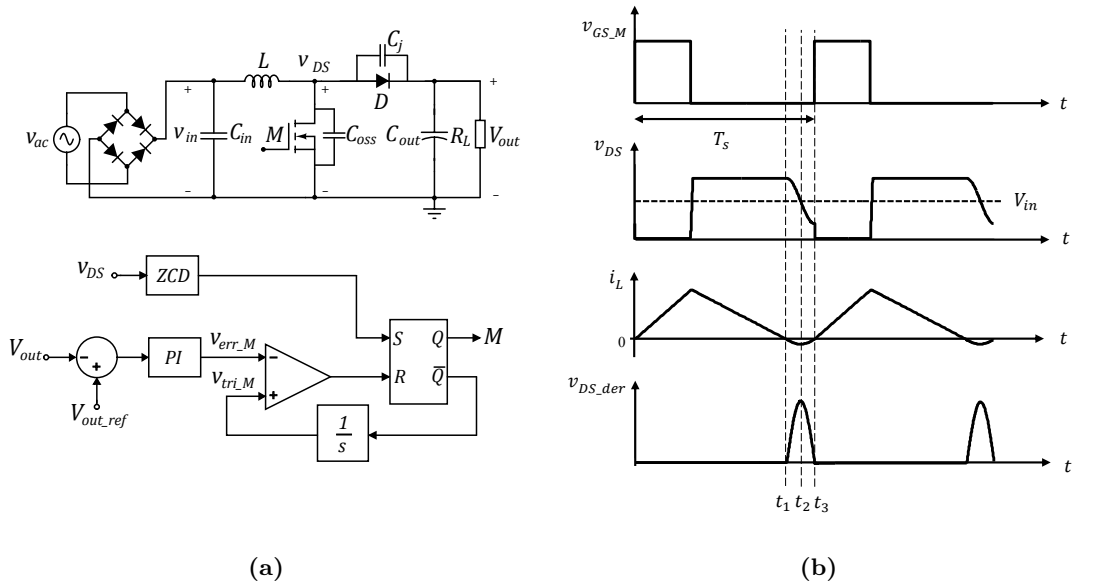


Figure 5.1: Ideal BCM inductor current waveform.

5.1 BCM with Valley/ZVS Switching Operation

Valley switching operation control is usually achieved by performing a comparison of the voltages across the converter inductor [94],[95],[96]. For example, in a boost converter as shown in Figure 5.2a, when the inductor current reaches zero value at t_1, the rectifier diode becomes reverse biased and the switching node voltage starts decreasing as seen



(a) **(b)**

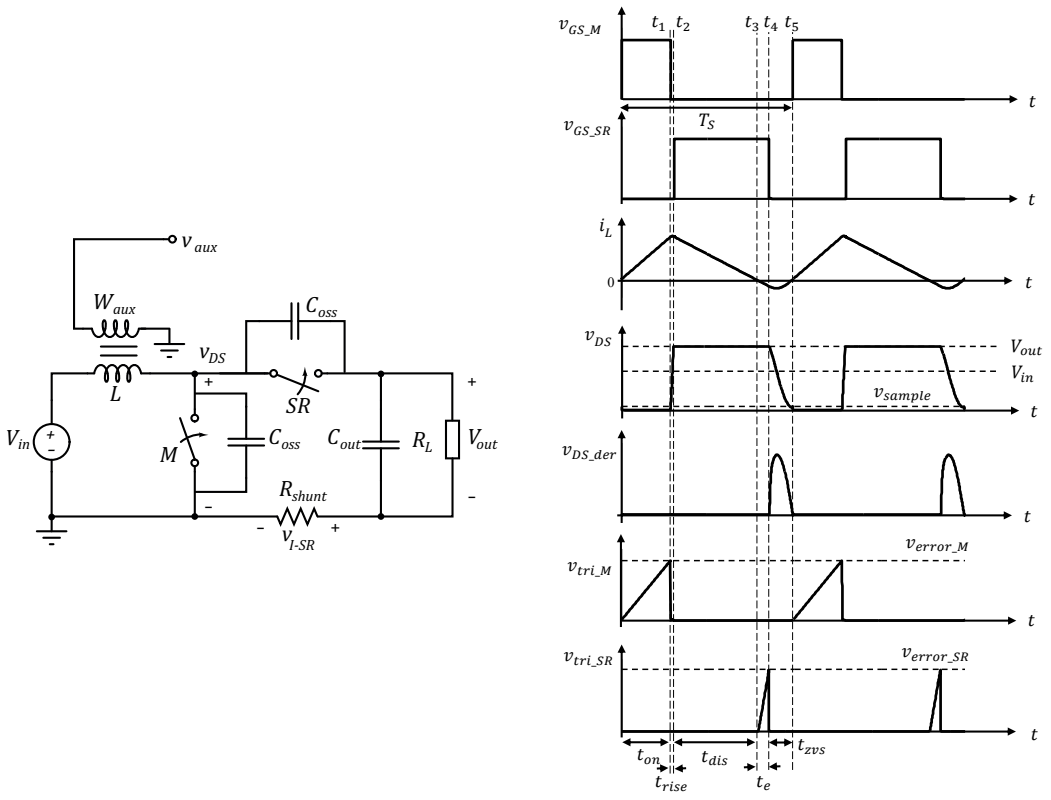
Figure 5.2: Boost converter with simmplified BCM control diagram (a) and BCM with valley switching key waveforms.

in Figure 5.2b. The turn-on instant is determined after waiting a fixed delay time after the converter switching node voltage level goes under the input voltage at t_2. This fixed delay time $(t_3 - t_2)$ is adjusted as $1/4 \cdot t_0$ where $t_0 = 1/2\pi\omega_0$ is the period of the resonant circuit formed by the switching node parasitic capacitance and the input inductor. However, due to the non-linear capacitance of the semiconductors connected to the switching node, the fixed delay time approach fails to achieve valley or ZVS under all input voltage v_{in} operating conditions. A variation of this control method uses the derivative of the switching node voltage v_{DS_der} as the control variable for determining the activation of the main switch [97]. As can be seen in Figure 5.2b, when the switching node voltage reaches the minimum voltage condition, the derivative of this voltage reaches zero volts indicating the turn-on instant of the switch.

5.2 Zero Voltage Switching Extension Method

The ability of the switching node to reach ZVS conditions in a BCM implementation depends on the converter operating voltages and the switching node capacitance variation as a function of the voltage. In a boost converter with a non varying linear capacitor attached to the switching node, the BCM converter will loose its ability to operate under ZVS conditions when $V_{in} \geq V_{out}/2$. However, as presented in [98] if a synchronous rectifier is used under BCM operation, it is possible to extend the ZVS conditions of the converter by letting the synchronous rectifier switch on after the inductor reaches zero current condition. In this way, if enough negative current is build in the converter inductor, the switching node voltage can be controlled to reach ZVS conditions independently of the instantaneous converter input to output voltage ratio. A BCM PFC converter using GaN cascode devices operating in the MHz switching frequency range is presented in [56]. All the work presented in the literature controls the synchronous rectifier extra conduction time after the inductor zero crossing detec-

tion by using curve fitting or look up tables created from experimental characterization. However, this control method based on characterization data is sensitive to components tolerance and variations in propagation delay times that may result in failure to achieve ZVS conditions or an increased components current stress. Appendix G presents an adaptive control method that adjusts the extra conduction time of the synchronous rectifier based on a closed loop control of the sampled switching node voltage. This control scheme is similar to the conventional BCM control method where the turn on instant of the main switch is determined by the derivative of the voltage of the switching node. As it can be seen in Figure 5.3a, the voltage across the converter input inductor is sensed with an auxiliary winding. This auxiliary winding voltage is used to reconstruct the converter switching node voltage waveform. Figure 5.3b shows the proposed control key operating waveforms and Figure 5.4 presents the control bloock diagram. When the derivative of the auxiliary winding voltage reaches zero volts, the first sample and hold cell S&H1 retains the reconstructed switching node voltage before turning on the main switch. The sampled value is sampled by the second sample and hold cell after the main switch has been turned on. The voltage in the second sample and hold cell is then a representation of the switching node voltage under valley switching conditions. This voltage is fed to a error amplifier that controls the synchronous rectifier extra conduction time to maintain a switching node voltage slightly higher than zero under valley switching conditions.



(a) **(b)**

Figure 5.3: Ideal boost converter with synchronous rectification (a) and Proposed ZVS control key waveforms.

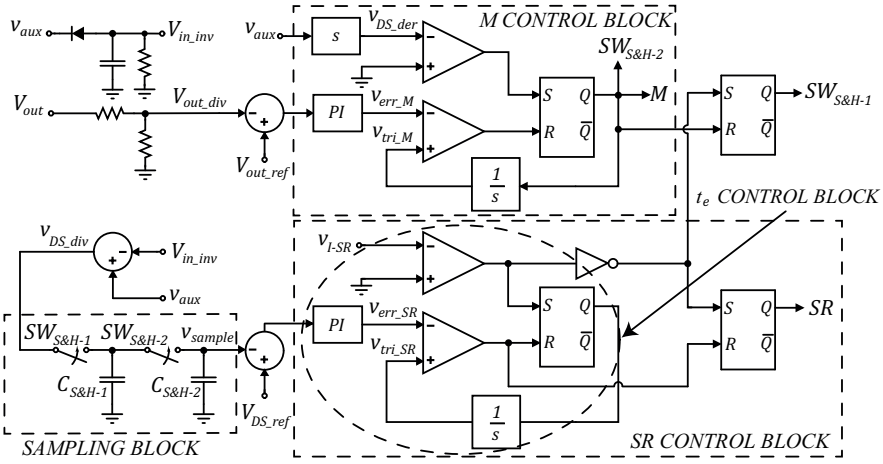
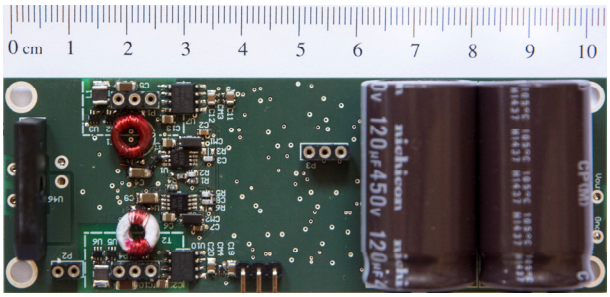
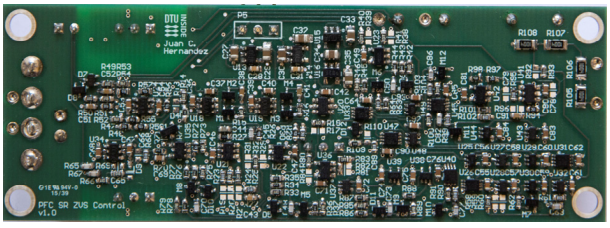


Figure 5.4: Proposed ZVS control block diagram.

Figure 5.5a and Figure 5.5b show the detailed top and bottom views of the implemented control board and Figure 5.6 shows the implemented PFC boost converter with the proposed control method. Figure 5.7 shows the converter operating waveforms under extended ZVS operation. The converter is operating with $V_{in} = 75\ V$ and $V_{out} = 110\ V$ and the extended time synchronous rectifier control loop is adjusted to regulate the switching node voltage $v_{DS}(t_5) = 10\ V$. As it can be seen, the first sample and hold cell retains the switching node voltage before turning on the main switch and the synchronous rectifier conduction is extended after the inductor current zero crossing condition. As demonstrated in Appendix G the control variable bahaves as a low order system with fast dynamics which makes the proposed control method able to regulate the switching node voltage under fast input voltage changing conditions in PFC applications.



(a)



(b)

Figure 5.5: Top (a) and bottom (b) views of the designed ZVS control PCB.

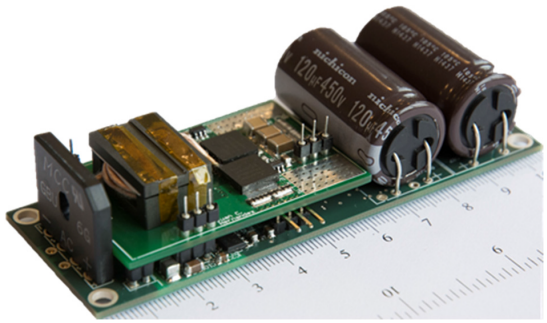


Figure 5.6: Integration of the proposed ZVS control and power stage PCBs.

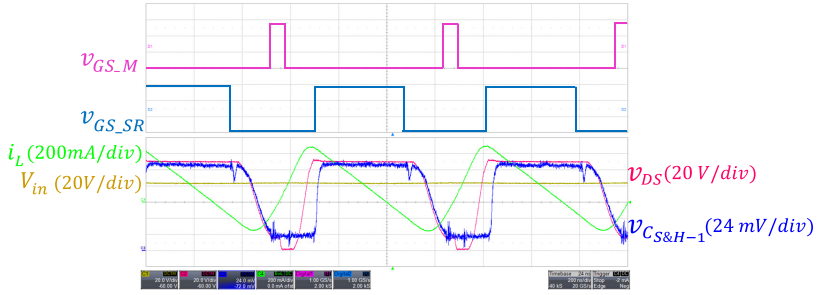


Figure 5.7: Converter operating waveforms under extended ZVS operation. Top digital channels: main switch gate signal v_{GS_M} and synchronous rectifier gate signal v_{GS_SR}. Bottom analog channels: converter input voltage v_{in} $(20V/div)$, converter switching node voltage v_{DS} $(20V/div)$, first sample and hold cell capacitor voltage $v_{C_{SH-1}}$ $(24\ mV/div)$, and inductor current $i_L(200\ mA/div)$. Time scale: 200 ns/div.

5.3 BCM, High frequency and GaN Implementation Challenges

BCM PFC converters with constant on time control suffer from input current distortion issues due to valley and switching frequency limitation operation [99]. The switching frequency limitation in BCM converters is often implemented to limit the converter operating frequency under light load conditions which limits the converter switching losses, and inductor copper and core losses. When the converter operates at low power conditions, the frequency will be clamped near the zero crossing of the input voltage waveform inserting distortion in the line current waveform. Moreover, the negative inductor current during valley switching operation makes the the average inductor current not proportional to the input voltage, which also inserts distortion in fixed on time BCM implementations. Several solutions have been proposed in the literature to address this issue. A variable on time control is proposed in [100], [49] where the fixed on time generated by the voltage loop error amplifier gets modified by adding a signal inversely proportional to the converter input voltage. However, due to the non-linear dependence between the correction signal and the converter input voltage, these type of implementations can not completely compensate the valley switching distortion unless a digital signal processor (DSP) is used. A control scheme similar to that used in

conventional CCM implementations is used in [101] to further reduce the distortion in the converter input current.

BCM implementations are sensitive to propagation delay times that result in increased capacitive switching losses. If a valley switching control method that determines the turn on of the main switch with the derivative of the switching node voltage is used, the propagation delay time from the zero derivative detection until the switch is turned on will produce the switching node voltage to increase resulting in increased switching losses. A control method is proposed in [96],[102] remove the propagation delay issues in BCM valley and ZVS operated converters.

Power semiconductor with low parasitic capacitances produce very fast switching transients with large *dv/dt*. Implementation of a high side gate drive for a fast switching GaN device is challenging due to propagation delay times and *dv/dt* noise immunity. A comparison between isolated high side gate drive solutions is performed in[103] where 150 V/ns safe operation of a high side drive isolator is demonstrated with good PCB practices to minimize parasitic coupling across both sides in the isolator.

The prototype implemented in Appendix G uses low propagation delay capacitive couplers (Si8610 with 10 ns typical propagation delay) with discrete low interwinding capacitance transformers and fast gate drive integrated circuits (UCC27511 with 13 ns typical propagation delay). Safe operation is observed, however, the propagation delay times of the digital isolators and the gate drivers represent an issue in MHz switching frequency implementations increasing the capacitive switching loss and the synchronous rectifier conduction loss. A control method to eliminate propagation delay issues as presented in [102] has to be investigated to allow high frequency BCM implementations.

6

Conclusion and Future Work

The goal of the PhD project "Single phase PFC converter using wide band-gap devices" was to study the possible attainable advantages that could be obtained by replacing current Si devices with wide band-gap semiconductors. Single phase PFC applications require semiconductor devices in the 600 V range. Vertical superjunction structures represent the state-of-the-art Si technology in this voltage range, while GaN seems to be the wide band-gap material for replacement of Si in this voltage range due to a reduced cost compared to SiC. Normally-off GaN devices are available nowadays in the 600 V range, however, during the duration of this PhD project, the only available devices were normally-on GaN devices configured in a cascode structure with a low voltage Si MOSFET to produce a normally-off device. All the work presented in this research project is based on evaluation and comparison between GaN cascode HEMT devices and Si superjunction MOSFETs. The main research areas and conclusions from this work can be summarized as:

- A characterization of state-of-the-art Si superjunction devices is performed to select a reference for comparison with GaN semiconductors. The characterization is based on DPT measurements for switching loss evaluation and parasitic capacitance measurements to estimate the devices performance in resonant applications. The results from the switching loss characterization show small differences in energy loss between the evaluated Si and GaN switches, but reveal a load current driven turn-off mechanism in the cascode GaN that makes this device a good candidate for BCM implementations. The parasitic capacitance measurement reveals a much larger capacitance charge for superjunction structures that puts this technology in disadvantage to GaN devices in resonant applications.

- The characterized devices are evaluated based on a mathematical model of a conventional boost PFC converter operating in CCM/DCM and BCM modes. The mathematical model, evaluates semiconductor loss based on the characterization data, input inductor volume based on the energy storage requirement in this component, and input filter size based on the input filter corner frequency requirement.

  - Conventional CCM implementations, are designed with switching frequencies close to $50, 75, 150$ kHz to reduce the converter input filter size by keeping up to the third, second and first harmonic of the converter switch-

ing frequency outside of the frequency measurement range specified by the standard. The evaluation, shows that a five times reduction of the input inductor size is possible under CCM operation with superjunction switches and SiC diodes, by increasing the converter switching frequency up to 350 kHz. This can be achieved without penalty on the input filter size compared to a CCM 45 kHz implementation. However, the semiconductor loss is increased 3.15 W or 0.6 % efficiency loss for a 500 W output power level.

  - The characterized GaN devices do not offer any performance improvement over the superjunction switches in CCM applications. However, a decreased semiconductor efficiency loss is possible in BCM implementations, due to the reduced capacitive switching loss under valley switching conditions and the load current driven turn-off mechanism.
  - BCM implementations offer a reduction in the input inductor size compared to CCM implementations, however, the input filter size can only be reduced compared to a 140 kHz CCM implementation when the converter switching frequency is pushed into the MHz operating range.

- BCM control schemes are investigated for implementation of a BCM operated MHz PFC converter. A new adaptive ZVS control method for BCM implementations is presented and demonstrated.

6.1 Future Work

Several aspects need to be further investigated in different areas:

- Dynamic on resistance and output capacitance series resistance have to be investigated and included into the characterization procedure to produce more accurate semiconductor models.
- Different magnetic structures need to be evaluated for MHz BCM implementations with custom made core shapes for reduced winding ac resistance.
- An inductor loss model and a thermal model for the PFC power stage needs to be developed to evaluate the accuracy of the implemented semiconductor evaluation model.
- A solution to the propagation delay times issues need to be implemented in the proposed BCM ZVS control by eliminating the isolators, investigating faster gate drive circuits or correcting for the delay in a closed loop control.
- Variable on time or current control methods need to be included in the BCM control schemes to reduce input current distortion.

7

Other Research Topics

This section presents other work carried out during this PhD project that are not related to the main topic.

7.1 Isolated boost converter with bidirectional operation for supercapacitor applications

Energy storage elements such as batteries and supercapacitors are often necessary in applications using renewable energy sources either to compensate for the intermittent power availability of the source, or to increase the system power density. An isolated bidirectional boost converter for regenerative braking applications is demonstrated in Appendix H where the state space modeling and control are analyzed, and safe start-up converter procedure is investigated. The converter bidirectional operation with batteries connected to both input ports, and a supercapacitor charge event under constant power operation are demonstrated.

7.2 Isolated boost converter with bidirectional operation for supercapacitor applications

A fuel cell battery charger based on primary parallel isolated boost converter topology is proposed in Appendix I. A new operation mode is proposed to extend the voltage operating range by short circuiting of the primary sides. This operation mode is useful in applications with wide variations in the converter output voltage.

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List of Publications

Appendix A

- Ultrafast Switching Superjunction MOSFETs for Single Phase PFC Applications.

Appendix B

- Switching Investigations on a SiC MOSFET in a TO-247 Package.

Appendix C

- Low Capacitive Inductors for Fast Switching Devices in Active Power Factor Correction Applications.

Appendix D

- Evaluation of 600V Superjunction Devices in Single Phase PFC Applications under CCM Operation.

Appendix E

- Characterization and Evaluation of 600 V Devices for Active Power Factor Correction in Boundary and Continuous Conduction. Modes

Appendix F

- A Comparison between Boundary and Continuous Conduction Modes in Single Phase PFC Using 600V Superjunction Devices.

Appendix G

- Zero Voltage Switching Control Method for MHz Gallium-Nitride based Boundary Conduction Mode Converters.

Appendix H

- Isolated Boost Converter with Bidirectional Operation for Supercapacitor Applications.

Appendix I

- Wide Operating Voltage Range Fuel Cell Battery Charger.

A

Ultrafast Switching Superjunction MOSFETs for Single Phase PFC Applications

2014 IEEE Applied Power Electronics Conference and Exposition (APEC 2014)

Ultrafast Switching Superjunction MOSFETs for Single Phase PFC Applications

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***Abstract*—This paper presents a guide on characterizing state-of-the-art silicon superjunction (SJ) devices in the 600V range for single phase power factor correction (PFC) applications. The characterization procedure is based on a minimally inductive double pulse tester (DPT) with a very low intrusive current measurement method, which enables reaching the switching speed limits of these devices. Due to the intrinsic low and non-linear capacitances in vertical SJ MOSFETs, special attention needs to be paid to the gate drive design to minimize oscillations and limit the maximum dv/dt at turn off. This paper investigates the latest SJ devices in order to set a reference for future research on improvement over silicon (Si) attained with the introduction of wide bandgap devices in single phase PFC applications. The obtained results show that the latest generation of SJ devices set a new benchmark for its wide bandgap competitors.**

I. INTRODUCTION

Power semiconductor devices in the 600V range are about to be replaced with new devices based on wide bandgap materials. As shown in Table I, Gallium Nitride (GaN) and Silicon Carbide (SiC) materials present higher electrical field strength and higher electron mobility compared to Silicon (Si). This allows for a reduction in the die size [1]. Moreover, these materials present a lower dielectric constant. This, coupled with the die size reduction, makes it possible to decrease the parasitic capacitances, directly enhancing the device switching performance.

Bulk GaN is an expensive material (100 €/cm^2) compared to SiC (10 €/cm^2) and Si (0.1 €/cm^2) [2]. However, epitaxial growth of GaN on Si substrate, together with higher electron mobility and electrical field strength compared to SiC, has made GaN devices to be an attractive solution in the 600V range.

On the other hand, Si based devices represent a very mature technology. This often overcomes the material disadvantages compared to wide bandgap devices, whose manufacturing processes are still far from reaching the theoretical material limits [3]. This paper investigates the dynamic performance of state-of-the-art Si devices in the 600V range for single phase PFC applications.

TABLE I
WIDE BANDGAP VS. SILICON PROPERTIES

Properties	Si	4H-SiC	GaN
Bandgap E_G [eV]	1.12	3.26	3.39
Critical field E_{crit} [MV/cm]	0.23	2.2	3.3
Thermal conductivity λ [W/cm·K]	1.5	3.8	1.3
Electron mobility μ [cm^2/V·s]	1500	650	2000

II. SUPERJUNCTION SI MOSFETS

Vertical SJ MOSFETs based on charge balance have set a new benchmark for high voltage Si devices, enabling a reduction of the on resistance and parasitic capacitances [4]. These switches are characterized by very low and highly nonlinear drain to source and drain to gate capacitances. These characteristics will produce extremely fast di/dt and dv/dt at turn off, with close to zero voltage switching (ZVS) operation when a low resistive/inductive gate drive circuit is employed [5], [6]. Under this condition the dv/dt will be determined by the current level, the circuit parasitic inductance and the charge of the MOSFET output capacitance. Exceeding the dv/dt can cause self-destruction due to the activation and thermal runaway of the parasitic bipolar junction transistor (BJT) [7]. This behavior is potentially dangerous in PFC circuits with average input current control, where a grid voltage transient can result in an abnormal inductor current level. The aforementioned issues are taken into account in the switching loss characterization to ensure that the maximum dv/dt ratings of the devices are not exceeded.

III. DOUBLE PULSE TESTER DESIGN

Printed circuit board (PCB) layout, package selection and other circuit parasitics are critical in modern power electronics [8]. Increasing the switching frequency to enable higher power densities is only possible under careful design of the PCB layout. A four layer PCB is used to reduce the area of the critical ac current loops. Special care has been taken to minimize parasitic inductances in the MOSFET and diode current paths as well as in the driving circuitry. Moreover, as proposed in [6], the capacitive coupling between drain and gate has been minimized to reduce gate oscillations.

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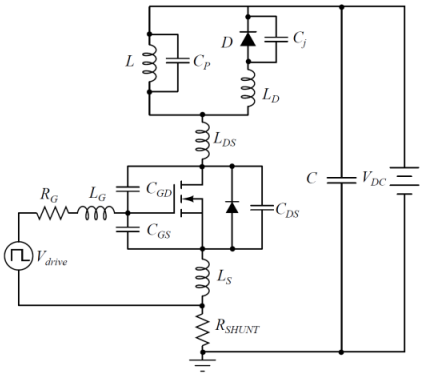

Figure 1. Double pulse tester schematic with components' parasitic capacitances

Fig. 1 shows the DPT schematic with the parasitic components. The PCB is designed to accommodate DPAK (TO-252) and leadless 8x8mm packages for the power MOSFET. DPAK and D^2PAK (TO-263) can be accommodated for the freewheeling diode. Flat mounted packages allow cancelling or reducing some of the package parasitic inductances and are preferred in this work.

In order to extract the switching energy, both voltage across and current through the device need to be measured. An overview of different current sensing solutions for integration in PCB or power modules is presented in [9]. One of the most adopted solutions is based on coaxial resistors [10]. State-of-the-art current measurement in high switching speed applications is based on the SDN coaxial current shunt series from T&M Research Products, claiming bandwidths up to 2GHz. This solution has been previously adopted for SiC and GaN characterization, as presented in [11] and [12]. However, due to the large parasitic inductance inserted in the loop by this device (2.2 nH [11]), the flat distributed shunt approach presented in [13] and [14] is used instead. This current shunt consists of an array of paralleled surface mount resistors (SMD). A pick-up wire placed as shown in Fig. 2, reduces the inductive coupling and increases the bandwidth of the measurement. However, as presented in [14], this shunt structure can present current distribution problems, limiting the accuracy and bandwidth of the current measurement. In order to overcome this problem, a high shunt resistance value is selected, which also reduces the inductive effect in the current measurement. The designed shunt structure is composed by 10x10Ω thin film resistors (0603 package) mounted in parallel. Since the resistive element in the resistor package is placed on top, these components are mounted upside down to reduce the distance from the resistive element to the PCB current return path. Fig.3 shows a Finite Element Analysis (FEA) of the current measurement structure to evaluate its bandwidth. The analysis shows that the bandwidth of the current measurement is well above B_ω= 500MHz. As presented in [15] and shown in Eq. (1), the obtained bandwidth makes it possible to measure signals with a rise time down to t_r = 0.7ns.

$$t_r = \frac{0.35}{B_\omega} \quad (1)$$

Fig. 4 shows the implemented DPT prototype with the integrated current shunt. The MOSFET driver used in this prototype is a 9A FAN3122 from Fairchild Semiconductor. Fig. 5 shows the designed low capacitive inductor. This component is implemented using two K6527E040 cores from Magnetics in a single layer configuration with a total magnetizing inductance of 213µH and a parasitic capacitance of 2.9pF.

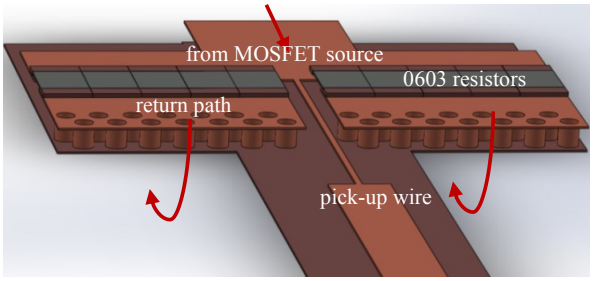

Figure 2. Integrated flat shunt 3D model used for FEA simulation

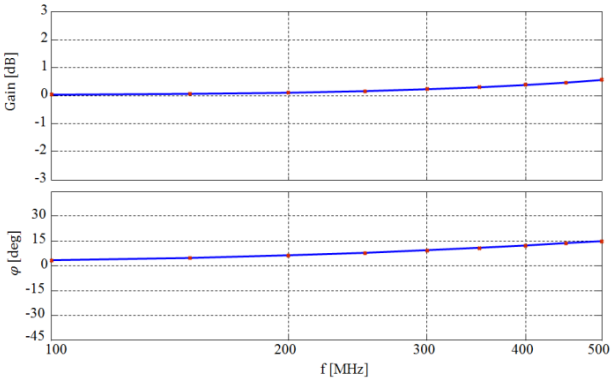

Figure 3. FEA current measurement transfer function

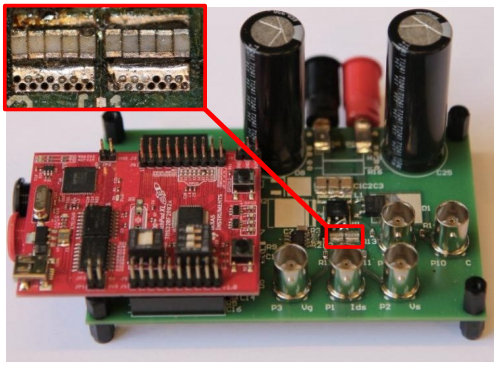

Figure 4. Double pulse tester prototype with integrated current shunt

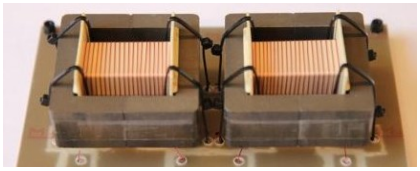

Figure 5. Low capacitance inductor prototype

IV. CHARACTERIZATION RESULTS

In this work, five SJ devices and six SiC diodes with different die sizes in the 600V range have been selected. The MOSFETs have been chosen based on their input gate charge and on resistance. Three of the devices (Fairchild and STMicroelectronics) are mounted in DPAK and the other two (Infineon C7) in a flat 8x8mm package with kelvin connection for the gate drive source. Table II shows the manufacturer specified gate charges and internal gate resistances together with the measured on resistance at 25°C. The SiC diodes are selected from two different manufacturers. The smaller die sizes are CREE C3D0X060E in 2, 3 and 4A versions, while the larger die sizes are Infineon IDDXXSG60C in 6, 8 and 10A versions. Fig. 6 presents the measured diodes' I-V curves at 25 °C.

The two smaller SJ devices (FCD9N60NTM and STD13NM60N) are characterized with the small CREE SiC diodes and the large die sizes with the Infineon SiC diodes.

The DPT prototype is based on the digital signal processor (DSP) evaluation platform C2000™ Piccolo Launchpad. An automatic characterization procedure has been developed. The switching waveforms are automatically saved on each trigger event and post processed using MATLAB. Switching energy, voltage and current derivatives for different inductor current levels are extracted. Fig. 7 and Fig. 8 show the DPT turn on and turn off waveforms with a 5 ns time scale. Fig. 9 and Fig. 10 show the post processed voltage and current waveforms for different inductor current levels.

TABLE II
CHARACTERIZED SUPERJUNCTION DEVICES

Device	V_{DSS} [V]	R_{DS} @ 25°C [mΩ]	Q_G [nC]	R_g [Ω]
FCD9N60NTM	600	391	18 @ V_{GS} = 10V & V_{DS} = 380V	-
STD13NM60N	600	348	27 @ V_{GS} =10V & V_{DS} = 480 V	4.7
STD18N65M5	650	182	31 @ V_{GS} =10V & V_{DS} = 520V	3
65R230C7	650	231	20 @ V_{GS} =10V & V_{DS} =400V	1
65R130C7	650	118	35 @ V_{GS}= 10V & V_{DS} = 400V	1

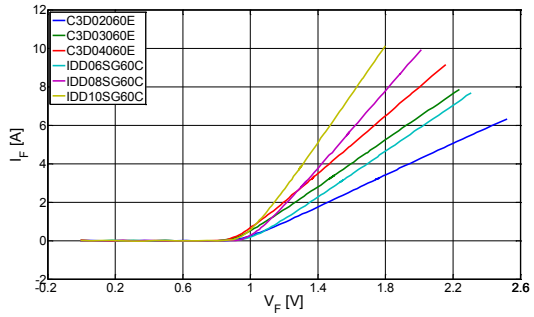

Figure 6. Diode V_F - I_F curves @ 25 °C

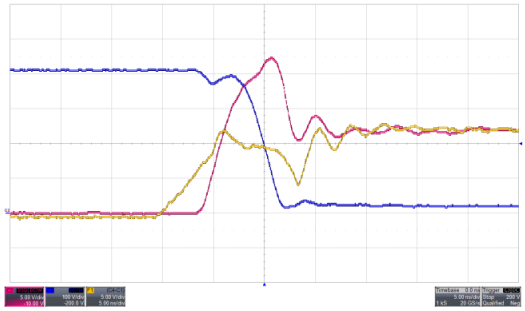
Figure 7. FCD9N60NTM and IDD10SG60C turn on waveforms. Light brown V_{GS} (5V/div), red I_D (5A/div), blue V_{DS} (100V/div). Time scale (5ns/div)

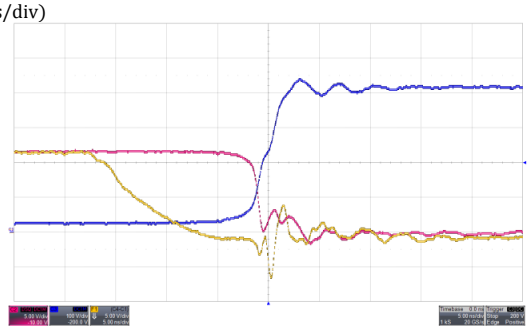
Figure 8. FCD9N60NTM and IDD10SG60C turn off waveforms. Light brown V_{GS} (5V/div), red I_D (5A/div), blue V_{DS} (100V/div). Time scale (5ns/div)

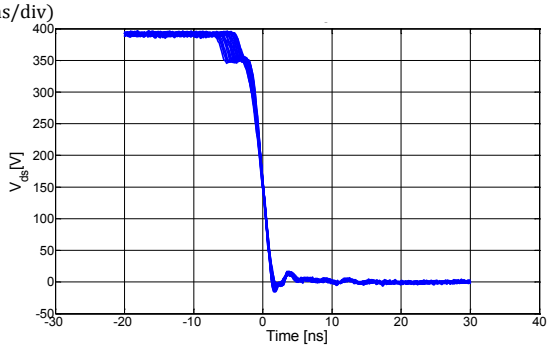

Figure 9. MOSFET drain to source voltage waveform during turn on for different inductor current levels

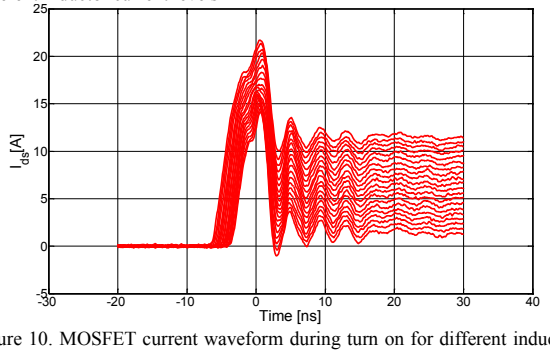

Figure 10. MOSFET current waveform during turn on for different inductor current levels

The switching waveforms are measured for different current levels, gate resistances and devices' junction temperatures. The junction temperature is controlled by a hot plate with temperature control based on thermocouple feedback. In this way it is possible to create a 4D space

solution for the devices' turn on and turn off energy loss and V_{DS} voltage derivatives. In this research, the effect of the gate resistance on the maximum dv/dt at the turn off of the MOSFET is considered. As presented in [6], due to the large MOSFET output capacitance at low voltage levels, SJ devices will exhibit a quasi ZVS (QZVS) behavior when very low gate resistance is used in the drive circuitry. Under these conditions, the current will be removed from the MOSFET channel under almost zero voltage conditions and the gate drive will not be in control of the device's dv/dt (now limited by the inductor current level and the device output capacitance value).

SJ manufacturers often specify the MOSFET dv/dt ruggedness rating related to BJT parasitic activation and gate activation by the C_{GD} charge at the MOSFET turn off. Moreover, as shown in [16], degraded blocking voltage capabilities were observed in the first generations of SiC diodes. However, as presented in [17], [18] and [19], these issues have been solved and reliability reports show safe operation over 100V/ns. Therefore, in this characterization the gate resistance at turn off will be adjusted to limit the maximum dv/dt to 100V/ns, regardless of the inductor current level. As shown in Fig. 11, a QZVS behavior is observed for 0Ω gate resistance with a switching energy loss corresponding to the MOSFET's output capacitance charge.

Fig. 12 and Fig. 13 show the instantaneous di/dt and dv/dt slope at turn off. When the gate resistance is equal to zero, it can be seen that the dv/dt only depends on the inductor current level. However, when the gate resistance is increased, the dv/dt is limited by the gate turn off speed. Fig. 14 shows the negative dv/dt slope dependence with the junction temperature. Fig. 15 shows a contour plot of the dv/dt slope vs. inductor current and gate resistance. Thus, the minimum gate resistance that limits the dv/dt can be obtained. Afterwards, the switching energy loss at turn off can be calculated by performing a 2D interpolation of the switching energy surface as a function of the gate resistance and inductor current level as shown in Fig. 16.

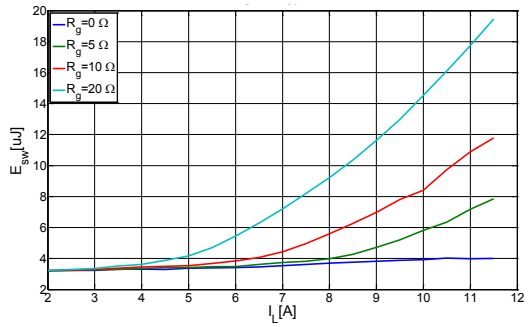

Figure 11. FCD9N60NTM and C3D02060E turn off energy loss vs. inductor current level for different gate resistances

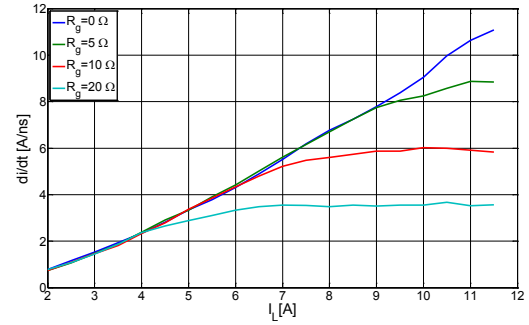

Figure 12. FCD9N60NTM and C3D02060E maximum instantaneous di/dt at turn off vs. inductor current level for different gate resistances

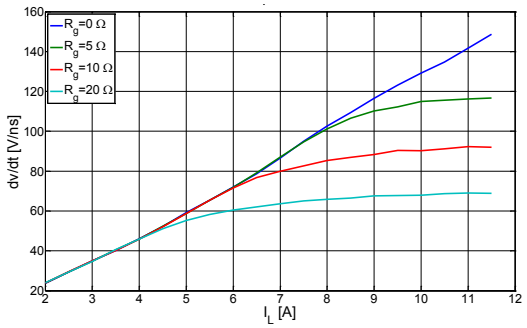

Figure 13. FCD9N60NTM and C3D02060E dv/dt slope at turn off vs. inductor current level for different gate resistances

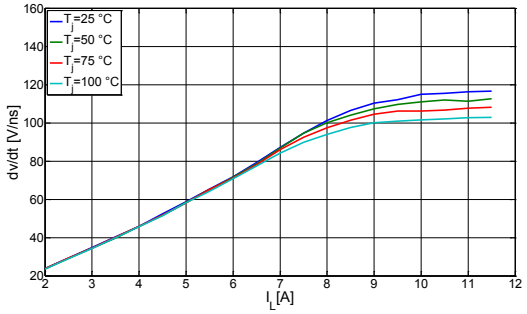

Figure 14. FCD9N60NTM and C3D02060E dv/dt slope at turn off vs. inductor current level for different junction temperatures

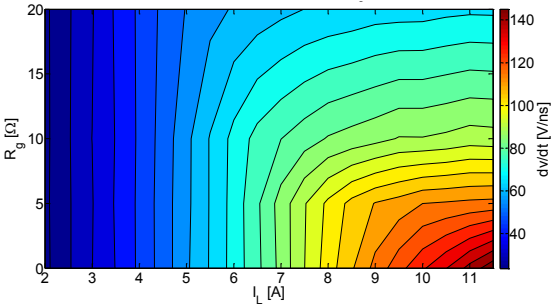

Figure 15. FCD9N60NTM and C3D02060E dv/dt at turn off vs. inductor current level as a function of the gate resistance

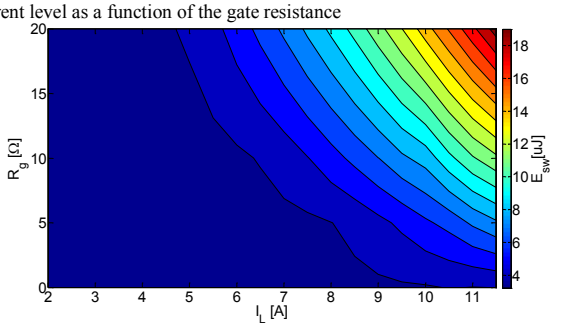

Figure 16. FCD9N60NTM and C3D02060E turn off energy loss vs. inductor current level as a function of the gate resistance

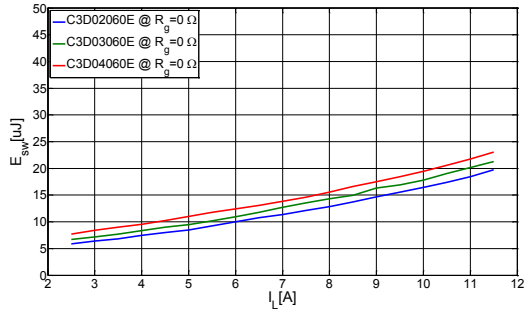

Figure 17. FCD9N60NTM turn on energy loss vs. inductor current level

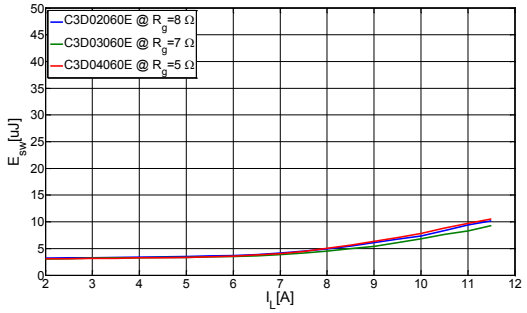

Figure 18. FCD9N60NTM turn off energy loss vs. inductor current level

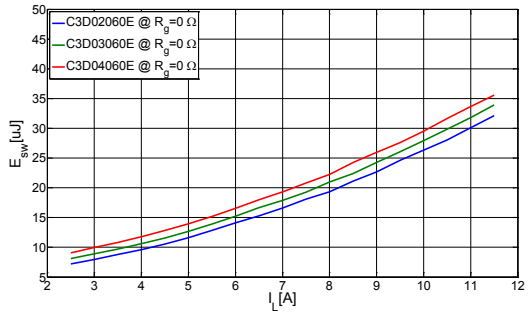

Figure 19. STD13NM60N turn on energy loss vs. inductor current level

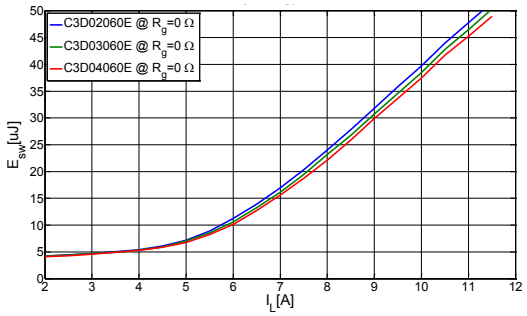

Figure 20. STD13NM60N turn off energy loss vs. inductor current level

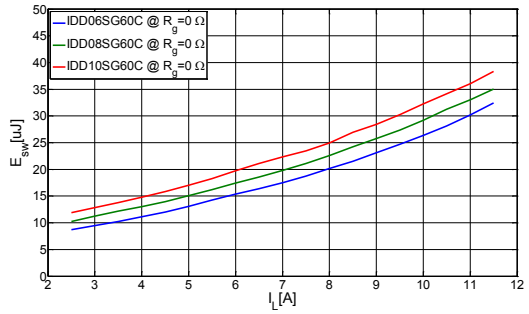

Figure 21. STD18N65M5 turn on energy loss vs. inductor current level

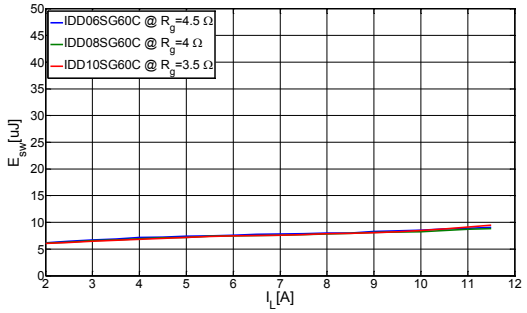

Figure 22. STD18N65M5 turn off energy loss vs. inductor current level

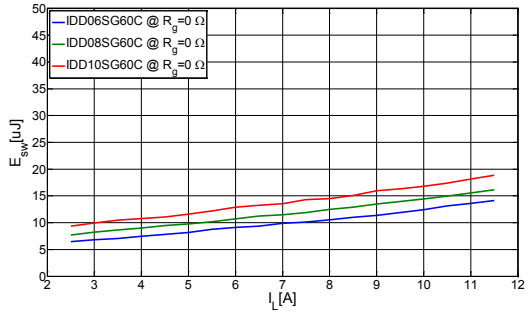

Figure 23. 65R230C7 turn on energy loss vs. inductor current level

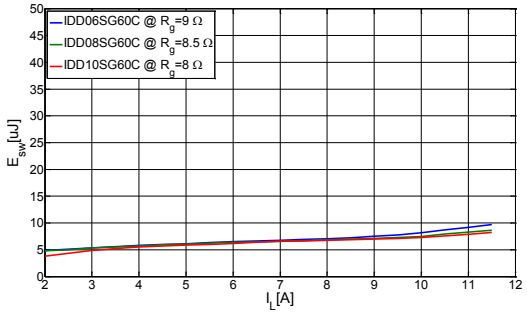

Figure 24. 65R230C7 turn off energy loss vs. inductor current level

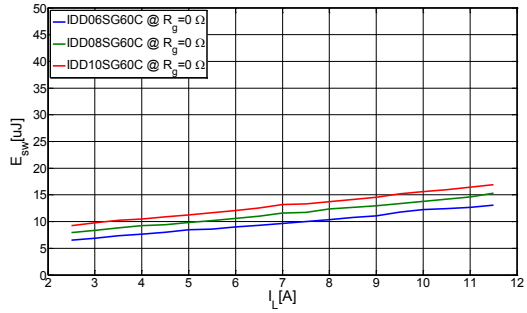

Figure 25. 65R130C7 turn on energy loss vs. inductor current level

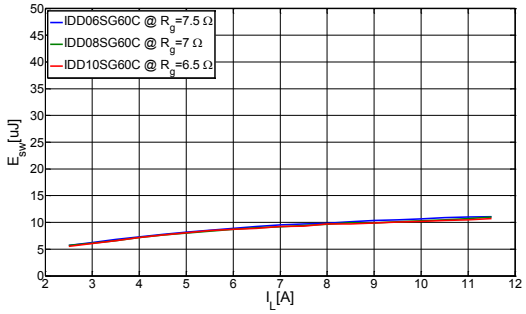

Figure 26. 65R130C7 turn off energy loss vs. inductor current level

Fig. 17 to Fig. 26 show the characterization results for the different analyzed SJ and SiC devices at a junction temperature of 25°C. The turn on loss energy curves are obtained at 0Ω gate resistance. The turn off loss corresponds to the calculated-interpolated gate resistance values in order not to exceed 100V/ns at turn off.

The difference in the diode junction capacitance charge can be observed in the turn on energy loss of the different MOSFETs, where the energy difference between the different diodes measurements is constant and independent of the current level.

From Fig. 20 it can be observed that MOSFET STD13NM60N is turned off with 0Ω gate resistance. This is due to the large internal gate resistance of the device (4.7Ω), which limits the maximum dv/dt to 35V/ns and has a negative effect on the switching loss.

The results obtained for the smallest device (FCD9N60NTM) show very low energy loss at both turn on and turn off. More remarkable are the results from the C7 devices from Infineon. It can be observed that the 65R130C7 presents lower turn on losses compared to the smaller 65230C7 device. In fact, attending to the results from the device 65R130C7, the obtained turn on losses for a 130mΩ are quite remarkable. This device in combination with the 6A diode from Infineon (IDD06SG60C Q_C =8nC at 400V) presents a lower turn on loss than the Fairchild device with the 4A diode from Cree (C3D04060E Q_C =8.5nC at 600V). This result can be compared with the results obtained in [20] corresponding to a 600V GaN High-Electron-Mobility-Transistor (HEMT) in cascode configuration with 150mΩ on resistance. In [20] the device switching energy is measured at dc voltage of 240V and a current range from 0 to 10A. The device measured in this work, 65R130C7 presents similar on resistance than the GaN device, but much smaller switching energy losses.

V. Discussion

The QZVS turn off capabilities of SJ devices need to be investigated as a very interesting feature for high frequency boundary conduction mode (BCM) operation in PFC applications. BCM makes possible to operate the switch under zero current switching (ZCS) conditions at turn on. If this operation is combined with a SJ device with 0Ω gate resistance and operated under QZVS conditions, the turn off energy loss will be independent of the current level.

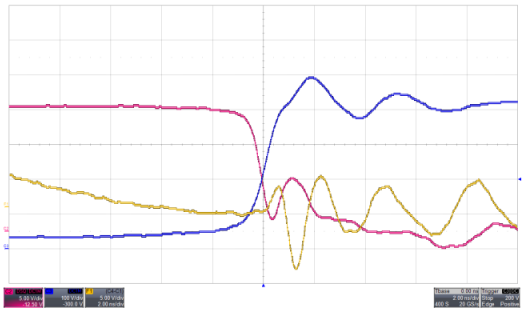

Figure 27. Turn off event FCD9N60NTM and C3D032060E. Light brown V_{GS} (5V/div), red I_D (5A/div), blue V_{DS} (100V/div). Time scale (2ns/div)

Is the author's experience that is possible to exceed the dv/dt manufacturer specified limits if a very low impedance gate drive is implemented to avoid gate activation due to the charge of the parasitic C_{GD} capacitance.

Fig. 27 shows a turn off event measured for FCD9N60NTM with CD032060E. In this experiment a 9A Zetex 3002 totem pole 9A driver was located in close proximity to the gate and source terminals to reduce the gate drive impedance. The inductor current level was increased until an absolute maximum dv/dt was found. The figure shows a drain to source voltage with a slope of more than 250V/ns on a 100V/ns rated device. (It is important to notice that this measurement may not represent the real waveforms due to the 500MHz bandwidth limitation of the oscilloscope voltage probes).

A last test was performed on FCD9N60NTM and CD032060E with a controlled junction temperature of 100°C. More than 10000 switch off events at 200V/ns dv/dt were measured without failure of the devices. These results are not concluding and more experiments need to be performed to clarify the device reliability when the maximum dv/dt is exceeded.

VI. Conclusion

This work evaluates state-of-the-art Si switches in the 600V range for single phase PFC applications setting a performance reference for the new wide bandgap materials. Several issues have to be addressed to ensure optimal switching performance. The DPT parasitic inductances and some of the packages' inductances are minimized by using a four layer

PCB design to minimize the ac current loops. Moreover a low intrusive current measurement method is used to minimize the insertion of parasitic inductances that would degrade the switching performance of the characterized devices.

The devices switching waveforms are saved and post processed in MATLAB to create a 4D map that can be used to calculate the switching energy and voltage derivatives by performing a curve fitting or a linear interpolation of the 4D space solution.

This work shows the obtained results for five SJ devices in combination with six different SiC diodes where dv/dt limitation at turn off has been taken into account to avoid parasitic BJT activation at turn off. The obtained results show that the latest SJ devices present very low switching energy loss together with a very low on resistance that makes these devices compete with some of the latest 600V GaN HEMT transistors.

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B

Switching Investigations on a SiC MOSFET in a TO-247 Package

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Switching Investigations on a SiC MOSFET in a TO-247 Package

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***Abstract*—This paper deals with the switching behavior of a SiC MOSFET in a TO-247 package. Based on simulations, critical parasitic inductances in the circuit layout are analyzed and their effect on the switching losses highlighted. Especially the common source inductance, a critical parameter in a TO-247 package, has a major influence on the switching energy. Crucial design guidelines for an improved double pulse test circuit are introduced which are used for practical investigations on the switching behavior. Switching energies of a SiC MOSFET in a TO-247 package is measured depending on varying gate resistance and loop inductances. With total switching energy of 340.24 µJ, the SiC MOSFET has more than six times lower switching losses than a regular Si IGBT. Implementing the SiC switches in a 3 kW T-Type inverter topology, efficiency improvements of 0.8 % are achieved and maximum efficiency of 97.7 % is reached.**

***Keywords*—SiC MOSFET, IGBT, multilevel inverter, Switching Energy**

I. Introduction

Silicon Carbide (SiC) devices have become more and more attractive in recent years by introducing SiC diodes which reduce stress on the main switching device due to the absence of reverse recovery current compared to Si diodes. One more way to increase efficiency in power converters is to replace Si switches by SiC switches such as SiC MOSFETs, SiC JFETs or SiC IGBTs. Their faster switching transitions compared to their Si counterparts enable possibilities to operate power converters at a high power density. Previous research has been done to investigate and utilize such devices in power converters in various applications [1]–[5]. Having fast switching transitions, a low parasitic printed circuit board (PCB) becomes more important. The purpose of this paper is to investigate the effect of parasitic elements in the circuit layout. Based on simulations, the influence of the PCB parasitic inductances on the switching energies is pointed out. A commonly used switching cell and PCB layout considerations optimized for fast switching transitions are introduced in order to limit such parasitic elements. Finally, on an optimized double pulse test (DPT) circuit, measurements on a SiC MOSFET in a TO-247 package are conducted in which switching energies are investigated relative to the gate resistance, the common source inductance as well as the junction capacitance of the freewheeling diode. Furthermore, the switching energies are compared to a Si IGBT. In Section II critical parasitic elements in a PCB circuit are investigated followed by a design guideline for PCB layouts with fast switching devices. The gate driver in the experimental setup is introduced in Section III. In Section IV, measurements on Cree's C2M0080120D SiC MOSFET are done showing switching behavior under different scenarios, e.g. varying gate resistance and stray inductance. Efficiency comparison of Si IGBTs and SiC MOSFETs in a 3 kW T-Type inverter are done in Section V. The conclusion is given in Section VI.

II. Double Pulse Tester

As the devices speed increase due to the reduced die parasitic capacitances, the circuit and package parasitic become more crucial in achieving the devices real performance. In this work, a DPT has been used for dynamic characterization. The double pulse tester is basically an inductor with a freewheeling diode that is used to evaluate the device under test (DUT) switching performance under clamped inductive load operation. The schematic of this circuit and the operating principle are shown in Fig. 1. At the instant t_1 the DUT is turned on and the inductor is charged up to the desired current level. At t_2 the DUT is turned off and the inductor current freewheels in the diode. At t_3 the DUT is turned on again and the turn on energy loss is measured by integrating the power in the switching interval. Finally the turn off energy loss is measured at the t_4 instant. The pattern is repeated for different current levels with a very low frequency repetition interval. In this way no self-heating effects are present and the characterization can be performed under controlled junction temperature conditions. The implemented prototype needs to offer flexibility and a modular design is preferred where different gate drive circuits can be tested by using a fast connection. The design is based on the digital signal processor (DSP) evaluation board C2000 Piccolo Launchpad. The implemented prototype is designed to accommodate a TO-247 for the switch and a TO-220 package for the diode. In order to extract the maximum switching performance of the evaluated devices, the DPT PCB design needs to be optimized. A Spice based simulation is used to evaluate the PCB parasitics impact on the device switching performance. The simulation circuit is constructed using a 1200 V, 20 A SiC MOSFET model from Cree Semiconductor *CMF20120* in TO-247 package and a 1200 V, 20 A SiC diode model from Rohm Semiconductor in TO-220 package. The simulation is implemented adding some PCB parasitics on top of the parasitics included in the models. The DPT with the circuit parasitic components is shown in Fig. 2. The simulation conditions are inductor current $I_L = 20\,\mathrm{A}$, supply voltage $V_{DC} = 800\,\mathrm{V}$ and gate drive voltage $V_{drive} = -5\,\mathrm{V}$ to $20\,\mathrm{V}$. Several simulations are performed varying the PCB parasitic

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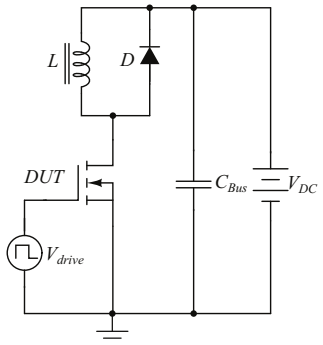
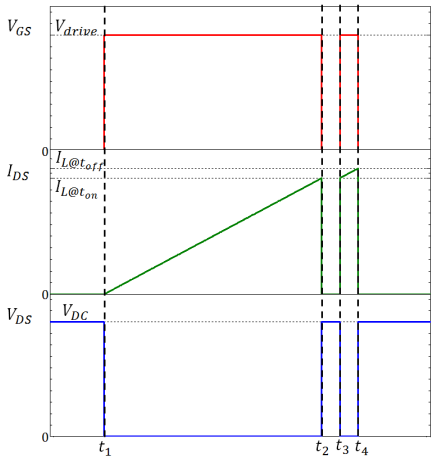


(a) Double pulse tester schematic



(b) Double pulse tester switching pattern

Fig. 1. Double pulse test circuit for evaluating switching performance of semiconductor power switches

inductances from 0 nH to 40 nH. The simulated turn on and turn off energy loss as well as the voltage overshoot at the DUT turn off event versus different parasitic inductances effects are shown in Fig. 3. According to the simulations, the gate drive inductance L_G does not have a remarkable effect on

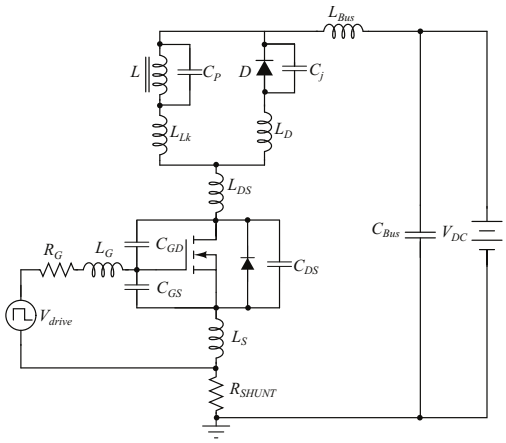
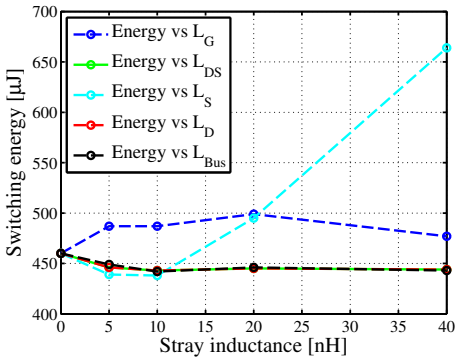
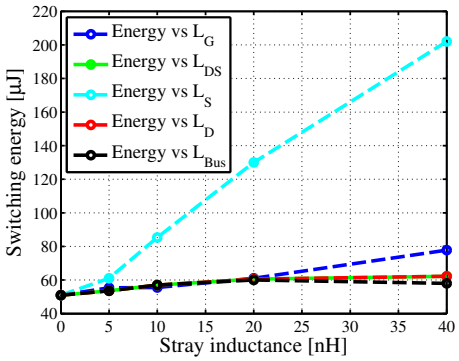


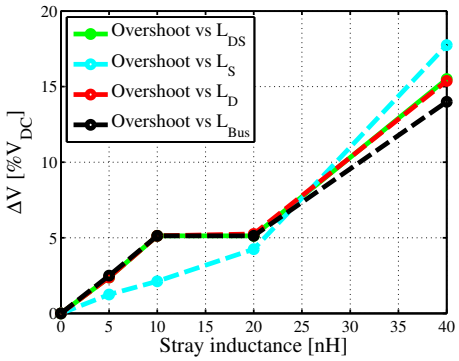
Fig. 2. Double pulse tester with parasitic components



(a) Simulated turn on energy loss vs. parasitic inductance



(b) Simulated turn off energy loss vs. parasitic inductance



(c) Simulated voltage overshoot vs. parasitic inductance

Fig. 3. Simulated switching energies and overshoot voltage on a non-ideal DPT

the device switching losses. During the turn on, the effect of this inductance will depend on the device threshold and the input gate charge. If these parameters are sufficiently large, the current through the driver loop parasitic inductance will build up before reaching the threshold voltage and the effect on the DUT switching energy will be minimal. The drain to source L_{DS} and diode L_D stray inductances do not increase the turn on loss and have a very small effect on the turn off energy loss that corresponds to the amount of stored energy on the stray fields when the DUT voltage reaches the supply voltage V_{DC}. In the same way, the supply loop stray inductance L_{Bus}

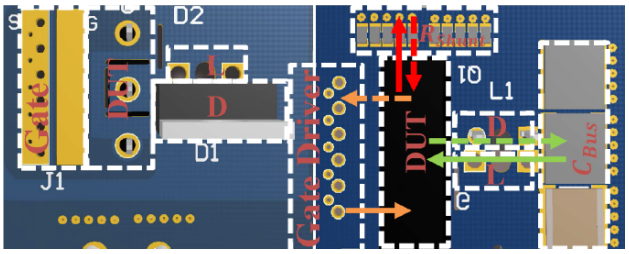


Fig. 4. DPT layout and current paths. Left (top view), right (bottom view)

will slightly reduce the turn on loss because it will create a voltage drop across the DUT, and will increase the turn off energy loss in a similar way to the loop inductances L_{DS} and L_D. However, the common source inductance L_S affects considerably the DUT switching energy both at turn on and at turn off. This parasitic element, shared between the power and driver loops produces a negative feedback Eq. (1) in the gate control signal when a high derivative is present in the current flowing through the switch.

$$V_{GS} = V_{drive} \pm L_S \frac{dI_{DS}}{dt} \tag{1}$$

The double pulse tester needs to be designed trying to minimize all the parasitic inductances, paying special attention to the common source inductance. The gate drive inductance needs to be minimized too because a low impedance gate drive circuit helps reducing parasitc gate activation due to current injection into the gate trough the C_{GD} capacitance at turn off. The implemented prototype uses a four layer PCB to increase the degrees of freedom in the design. The critical loop areas are minimized by implementing the current return paths (the arrows in Fig. 4 indicate the different current loops) in a contiguous layer. Capacitive coupling between drain to gate and gate to source is avoided and the capacitance of the switching node is minimized to avoid increasing the dissipated energy at turn on. Finally, the common source inductance effect due to the PCB is avoided by keeping the power loop current (green and red arrows) orthogonal to the driver loop current (orange arrows). The current measurement method selection is based on a study of state of the art techniques. Recent research work based on characterization of fast switching devices use coaxial current shunts [6]. These devices claim bandwidths up to 2 GHz and are very suitable for this work due to the fact that they only introduce 2 nH in the switching loop. In order to further reduce the inserted stray inductance in the loop, the current measurement proposed in [7] is implemented in this work. This current measurement technique has been previously used for characterizing high switching speed [8] devices and represents a non intrusive and low cost solution. The current measurement bandwidth is increased by decoupling the measurement from the inductive effect of the resistive structure. This is performed by using a pick up wire placed strategically in a low field intensity region. Moreover, the inductance of the structure is further reduced by mounting the resistors upside down in order to place the resistive element closer to the PCB to minimize the area of the current loop. The implemented current shunt structure is shown in Fig. 5.

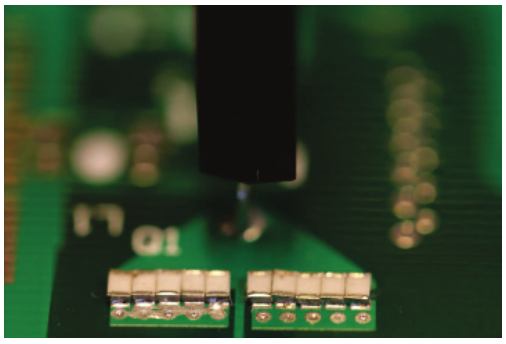


Fig. 5. Integrated flat current shunt

III. The Gate Driver

The gate driver used in this work comprises of a commercially available DC/DC converter, a digital isolator and a gate driver IC with a peak current capability of 9 A. The output of the DC/DC converter supplies ±15 V with a common ground on the secondary side. Two zener diodes are used to create the necessary voltage levels for the digital isolator as well as a reference voltage connected to the source terminal of the SiC MOSFET. An overview of the driver is shown in Fig. 6. With this constellation, the SiC MOSFET can be switched on with a positive voltage of 20.1 V and switched off with a negative voltage of –4.7 V.

IV. Practical Results

A. Low Side Measurements for Different Gate Resistances

Measurements on an optimized low side double pulse test circuit are conducted in order to investigate switching

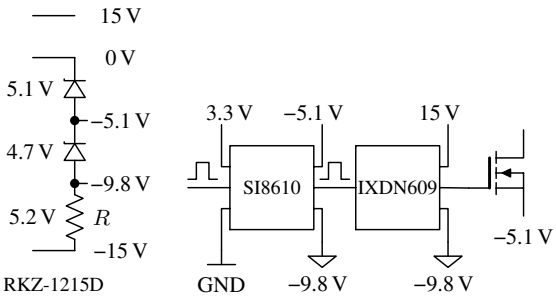


Fig. 6. Gate driver used for SiC MOSFETs

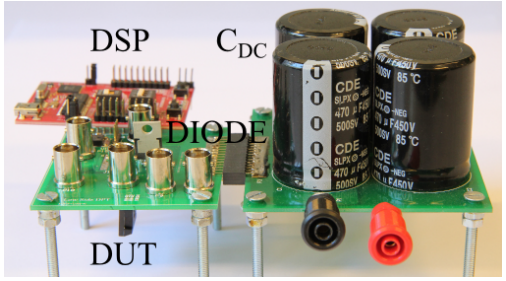
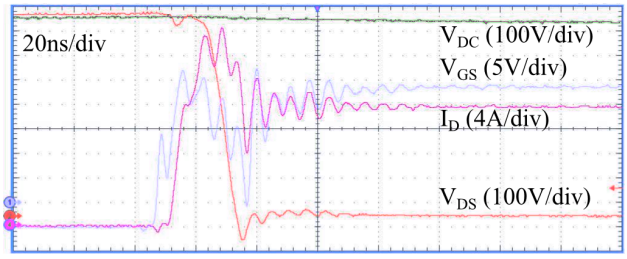
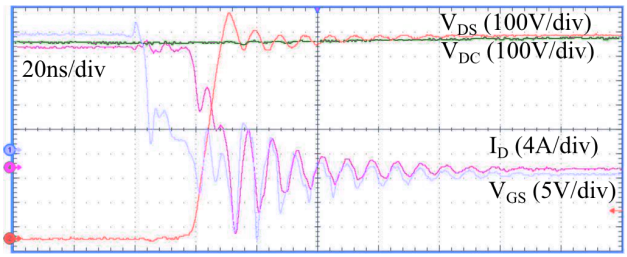


Fig. 7. Lab setup of the low side DPT



(a) Turn on transition



(b) Turn off transition

Fig. 8. Switching transition of a 1200 V SiC MOSFET in a double pulse test circuit. Gate resistance is 6 Ω

performance of SiC MOSFETs compared to varying gate resistors. The voltage probes in this work are Tektronix *P6139* (500 MHz) for the drain current and the gate to source voltage, and a Tektronix *P5100* (250 MHz) for the drain to source voltage. The DC link voltage is 800 V and the measured current range is from 5 A to 30 A. The setup can be seen in Fig. 7 and turn on and turn off transitions for a gate resistance of 6 Ω are shown in Fig. 8. Large oscillations in the gate to source voltage, the drain to source voltage as well as the drain current can be observed mainly due to the common source inductance of the TO-247 package. The resonance frequencies of the oscillations during turn on and turn off with SiC MOSFETs are 166.67 MHz and 125 MHz, respectively. The dv/dt for turn on and turn off are 84.6 V/ns and 85.88 V/ns. The di/dt is 8 A/ns and 1.33 A/ns for turn on and turn off, respectively. A common way to reduce and hence control the switching speeds is to increase the external gate resistance. The downside is an increase in switching energies due to the slower switching transitions. The switching energies for 0 Ω, 6 Ω and 12 Ω are

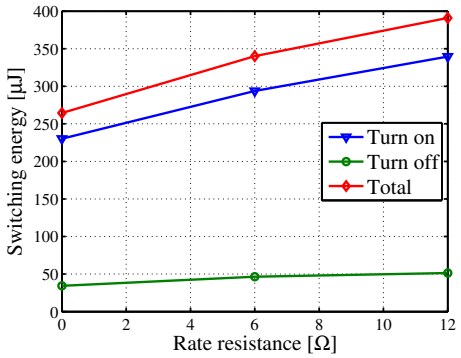
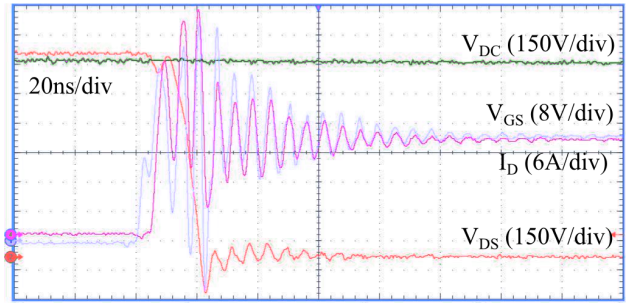
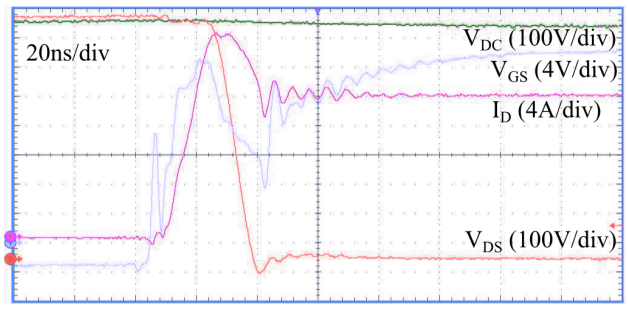


Fig. 9. Switching energies for different gate resistances



(a) Turn on transition for a gate resistance of 0 Ω



(b) Turn on transition for a gate resistance of 12 Ω

Fig. 10. Turn on transitions for different gate resistances

TABLE I. SEMICONDUCTOR COMPARISON

	$I_C/I_D[A]$	$Q_{Gate}[nC]$	$t_r[ns]$	$t_f[ns]$
IKW15N120T2	30	93	30	176
C2M0080120D	31.6	49.2	13.6	18.4

presented in Fig. 9. It can be seen that the turn on losses are mainly affected by an increased gate resistance whereas the turn off losses only slightly increase. A turn on switching comparison with 0 Ω and 12 Ω is shown in Fig. 10. Increasing the gate resistance reduces the peak gate current and hence the gate capacitance is charged slower such that the parasitics in the package as well as in the circuit become less critical. Especially the pointed out common source inductance shown in Eq. (1) has less influence.

B. Comparison to a Si IGBT

Commercially SiC switches come with a minimum breakdown voltage of 1200 V for different current ratings. Hence they are an alternative to replace 1200 V IGBTs in grid-tie applications, e.g. in photovoltaic systems, or motor drives. A comparison to a Si IGBT is conducted in order to see the reduction in switching energies. The chosen Si IGBT is Infineons IKW15N120T2, a second generation IGBT designed for frequency converters and uninterruptable power supplies. The main characteristics based on the semiconductor datasheets are listed in Table I. The same gate driver circuit as in Fig. 6 was used with the same voltage levels for turn on and turn off. Only the gate resistance was changed to 7 Ω in order to maintain the same peak gate current. The results can be seen in Fig. 11. Especially the turn off comparison shows the superior advantages of SiC MOSFETs over Si IGBTs due to the lack of the tail current. A total switching energy reduction of 84.2 % can be achieved at a switching current of 20 A.

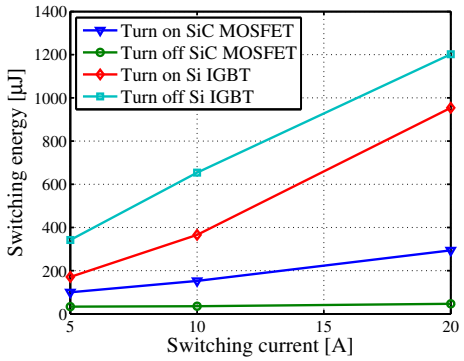
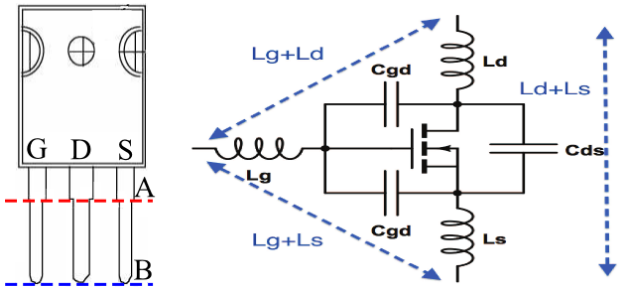


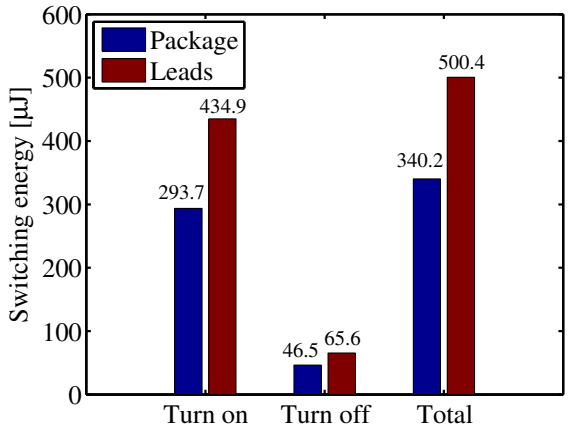
Fig. 11. Switching energy comparison between SiC MOSFET and Si IGBT

C. Effect of the lead inductance of the package

In the simulations, it is found out that the common-source inductance is a crucial aspect when it comes to switching energies. An increased inductance in the source path results in a larger switching energy loss. With an optimized PCB layout, the effect of the inductance of the leads of the TO-247 package is analyzed. A typical 1200 V switch in such package is shown in Fig. 12a and two kind of measurements were done. The first measurement represents the TO-247 SiC device being soldered to the DPT at the end of the leads (Point B, blue dotted line) from now on referred to as lifted leads. In the second measurement, the device is soldered to the DPT at the beginning of the leads (Point A, red dotted line). The comparison of these two scenarios with Cree's C2M0080120D SiC MOSFET is shown in Fig. 12b. It can be seen that having the TO-247 package soldered to the main PCB on Point A reduces the total switching energies by 32 %.



(a) Typical switch in a TO-247 package

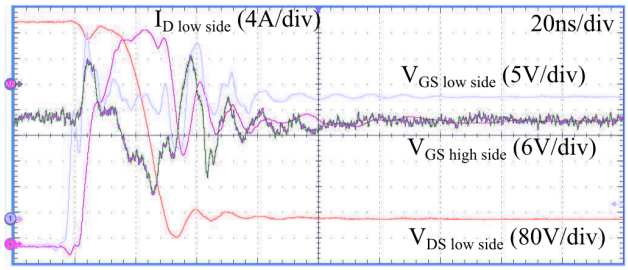


(b) Switching energies for different soldering points of the TO-247 package

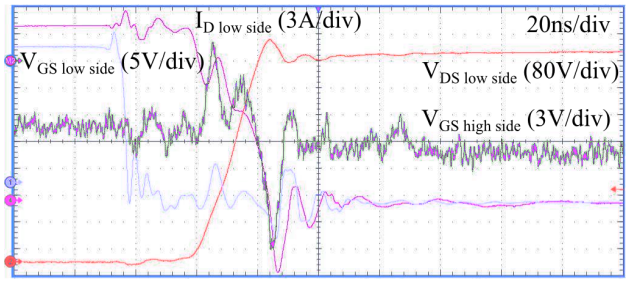
Fig. 12. Effect of the leads in a TO-247 package

D. Comparison of High Side Body Diode and Discrete SiC Diode

Until now, the DPT circuit comprised of a low side switch and a discrete SiC diode for free-wheeling the load current. A commonly encountered circuit configuration in power electronics is a phase leg comprising of a DC link voltage, a low side switch and a high side switch. Unlike Si IGBTs, SiC MOSFETs contain a parasitic body diode which can be used as a freewheeling diode. The effect of such body diode in the high side switch is investigated in this section and compared to a phase leg with an external SiC diode in parallel to the high side switch. Turn on and turn off transitions of the low side MOSFET as well as the gate to source voltage of the high side MOSFET are shown in Fig. 13. It can be seen that the gate to source voltage of the low side MOSFET is not dramatically affected by the switching transition. However, the gate to source voltage of the high side MOSFET is very much affected. By looking at the drain current through the low side MOSFET, it can be seen that no shoot through nor breakdown of the high side gate occurs. Comparing the switching energies of the low side MOSFET with a high side body diode and a discrete SiC diode, it can be seen that main efficiency improvements are achieved during the turn on process. At low current levels, the turn on energies using only the body diode presents the lowest losses because of the reduced parasitic capacitance. When an external SiC diode is used the increased



(a) Turn on transition



(b) Turn off transition

Fig. 13. Switching transition of a phase leg configuration

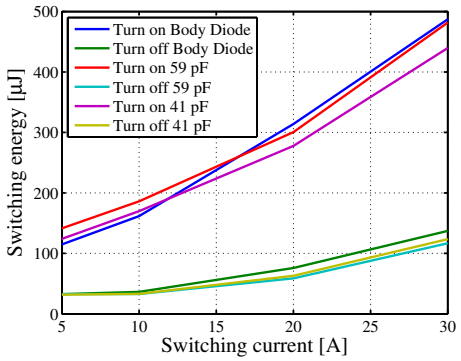


Fig. 14. Switching energies comparison for high side body diode and discrete SiC diodes

junction capacitance increases the losses at low current levels, however reduces the losses at high current levels because of the reduced reverse recovery effect in the body diode of the MOSFET. The turn off energies are less affected by the choice of discrete SiC diode or internal body diode as it can be seen in Fig. 14.

V. Efficiency Improvements Using SiC Switches

The effect of SiC switching devices is demonstrated on a 3 kW T-Type inverter whose schematic is shown in Fig. 15. It is a three level inverter topology that comprises of both 600 V and 1200 V semiconductor devices. More elaborated, switches S_3 and S_4 including their anti parallel diodes are 600 V devices because they have to withstand half the DC link voltage whereas S_1 and S_2 including their freewheeling diodes must be 1200 V devices because they have to block the whole DC link voltage. Furthermore, S_1 and S_2 are modulating the converter output voltage with a chosen switching frequency; typical values for residential photovoltaic applications are up to 20 kHz when Si IGBTs are used. The specifications are shown in Table II. A prototype of the T-Type inverter is designed according to the results and PCB guidelines in Section II in order to minimize the common-source inductance. Also, the switching devices are soldered to the PCB with a

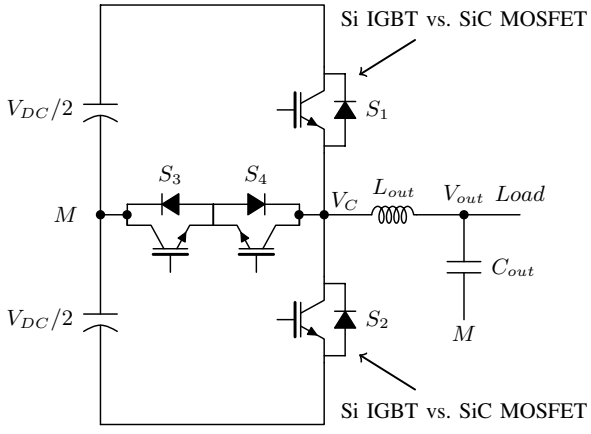
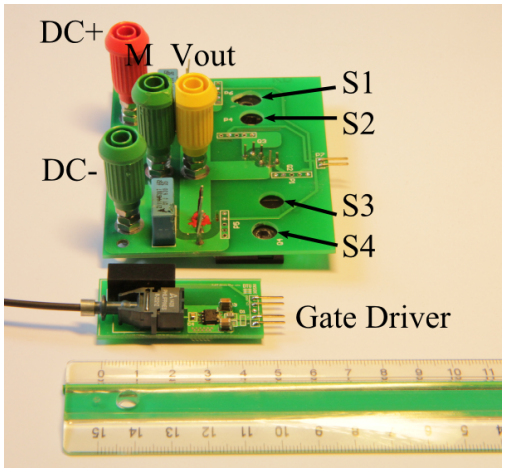


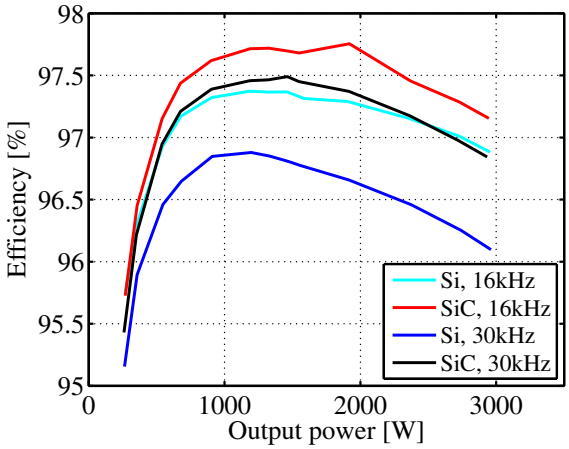
Fig. 15. T-Type inverter topology

TABLE II. Specifications

Symbol	Meaning	Value
L_{out}	Output filter inductance	3 mH
C_{out}	Output filter capacitance	4.4 µF
V_{DC}	DC link voltage	800 V
V_{out}	Filtered output voltage, RMS	230 V
P_{out}	Output power	250 W to 3000 W



(a) 3 kW prototype of T-Type inverter



(b) Efficiency improvements with SiC MOSFETs

Fig. 16. Prototype in (a) and measured efficiencies in (b)

minimum lead lengths (Point A in Fig. 12). The prototype as well as the efficiency curves using a N4L PPA5500 power analyzer for both the Si IGBT (IKW15N120T2) and the SiC MOSFET (C2M0080120D) version are shown in Fig. 16. Maximum efficiency improvements of 0.3 % are achieved at a switching frequency of 16 kHz. However, the benefits of the SiC switches become more visible as the switching frequency is increased up to 30 kHz. Maximum efficiency improvements at that switching frequency is then up to 0.8 %. According to the measurement results, the SiC based T-Type inverter at 30 kHz achieves similar efficiencies than the Si IGBT based inverter at 16 kHz.

VI. Conclusion

In this paper, switching performance of a commercially available SiC MOSFET has been investigated on a low parasitic DPT. Simulations have shown that the common source inductance has a significant negative impact on the switching losses. PCB design recommendations have been pointed out how to minimize such parasitic. In an optimized DPT circuit, a SiC MOSFET in a TO-247 package was evaluated based on different gate resistances. Even though the DPT is optimized for a low common source inductance, large oscillations are present due to the package parasitics. With a gate resistance of 6 Ω and a trade off between switching energy and oscillations, the SiC MOSFET has switching energies of 84.2 % lower than a Si IGBT. It is furthermore pointed out that the reverse recovery effect of the body diode of the high side MOSFET has a strong influence on the switching energies at higher current levels. Furthermore, it is recommended to use an external SiC diode with a low junction capacitance instead of using the body diode of the SiC MOSFET. Having SiC MOSFETs equipped in a 3 kW T-Type inverter, efficiencies could be increased by 0.8 % compared to a Si IGBTs counterpart.

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C

Low Capacitive Inductors for Fast Switching Devices in Active Power Factor Correction Applications

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Low Capacitive Inductors for Fast Switching Devices in Active Power Factor Correction Applications

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***Abstract*-This paper examines different winding strategies for reduced capacitance inductors in active power factor correction circuits (PFC). The effect of the parasitic capacitance is analyzed from an electro magnetic compatibility (EMI) and efficiency point of views. The purpose of this work is to investigate different winding approaches and identify suitable solutions for high switching frequency/high speed transition PFC designs. A low parasitic capacitance PCB based inductor design is proposed to address the challenges imposed by high switching frequency PFC Boost converters**

Keywords— Parasitic capacitance, PFC, boundary conduction mode (BCM), high frequency.

I. INTRODUCTION

Increased switching frequency operation in power electronics converters permit achieving high power densities due to the size reduction of the energy storage elements in the circuit. Resonant converters have been a common approach to overcome the reduced switching speeds in the active devices, making possible to mitigate or completely eliminate the switching losses present in hard switching topologies. On the other hand, a new era in power electronics is approaching and starting to be a reality with the introduction of wide bandgap devices based on silicon carbide (SiC) and gallium nitride (GaN) materials. The increased electrical strength and electrical conductivity in these materials allows for a reduction of the switch die size, consequently reducing the device parasitic capacitance, which directly increases the achievable switching speed of these devices. Previous works have proven the advantages of the utilization of wide bandgap devices, [1], [2]. However, increased hard switched converter operating switching frequencies requires more attention to be put into the printed circuit board (PCB) and magnetic components design in order to minimize the introduction of parasitic inductances and capacitances into the circuit.

The work presented in this paper focuses on the reduction of the parasitic capacitances of the PFC input inductor. Some research has already been performed on parasitic capacitance calculations based on analytical models [3], [4], [5] and finite element analysis [6]. The solution presented in [7] and [8] proposes a new winding strategy for reduction of inductors self-capacitance for SiC based power converters. A model for calculating the parasitic capacitance is addressed, and finally the effect of the reduction of this parasitic component is analyzed based on several measurements performed with different SiC devices. Some research has already been performed on the inductor self-capacitance effect on boost PFC's EMI performance. This work is part of a larger research project where the goal is to successfully introduce and take advantage of wide band gap devices for single phase PFC converters. It is the authors' opinion that this implicit means that the switching frequency must be increased in order to fully take advantage of these new devices. The justification of this paper is the work done on comparing different winding strategies in terms of EMI, switching and conduction loss. Furthermore, a novel winding strategy based on PCB manufacturing for reduced cost inductors with low ac resistance and self-capacitance is proposed. The proposed solution addresses the requirements for inductor designs in high frequency boost derived PFC circuits.

II. INDUCTOR PARALLEL CAPACITANCE

The inductor behavior at very high frequencies is clearly dominated by the parasitic capacitance effect and other non-ideal behavior. The component impedance can be approximated based on lumped parasitic models, which can be simplified to the model shown in Fig. 1.

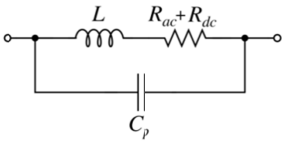

Fig. 1 Inductor equivalent simplified model

This model, presented in [9], includes the windings dc and ac resistances, which will effectively affect impedance curve quality factor at the component resonant frequencies. A parallel resistor, modeling the inductor core loss, is included in [10]. A more complex model based on impedance measurement fitting is presented in [11] and [12], in order to take into account very high frequency parasitic effects.

As presented in [7] and [8], if the capacitance has to be minimized, the layer to layer, the first turn to last turn and the turn to core capacitances represent the mayor contribution to the final capacitance of the inductor. This is due to the fact that even if the turn to turn capacitance is larger than the last ones, they will be interconnected in series minimizing its effect.

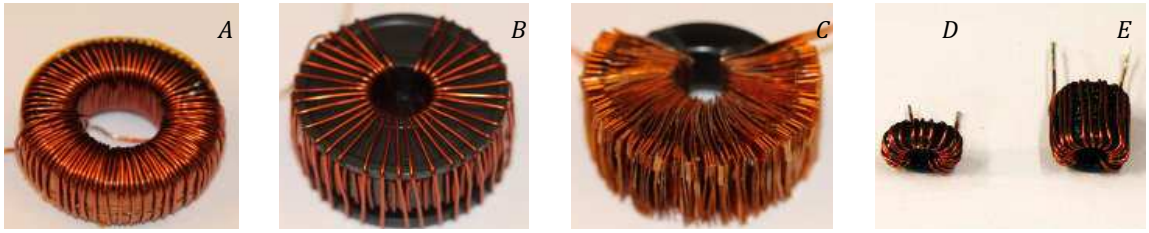

Fig. 2. Implemented inductor prototypes. A-Conventional double layer, B-Double layer with separator, C-Copper foil, Small size low capacitance inductors D-25 μH and E-69 μH.

III. Prototype Implementation

In order to compare the performance of different winding strategies, a toroidal Kool Mu core from Magnetics is selected. The same copper cross section and number of turns is used in all the implemented prototypes, to perform a fair comparison between the different winding structures. Toroidal cores are selected because they provide a large winding area compared to the core volume and represent a low cost solution in PFC inductor implementation. A first prototype is implemented using a conventional two layer structure that will present very large capacitance due to the layer-to- layer capacitance contribution. The selected core is 0077439A7 Kool Mμ 60 from Magnetics®. The winding is implemented using 94 turns of AWG 18 coated cable obtaining an inductance value of 1.2 mH. The well-known progressive winding or sectioned bobbin techniques [13] for reducing self-capacitance are not considered because of the difficulty of implementation in toroidal shaped cores. Instead, based on the work presented in [7] and [8], a two layer toroidal core with a layer to layer separator is implemented for layer-to-layer capacitance reduction. Moreover, a gap is introduced from first to last turn in each of the layers for reduction of the parasitic capacitance. Finally, in order to evaluate the feasibility of introducing PCB windings for this design, a copper foil implementation is selected where the copper cross section is adjusted to match the AWG18 cross section. This structure will present a relatively large turn-to-turn capacitance due to the increased area of the equivalent capacitance plates as shown in (1). Where ε_r is the relative permittivity, A is the plate area and d is the distance between plates.

$$C = \varepsilon_r \cdot \varepsilon_0 \cdot \frac{A}{d} \qquad (1)$$

However this structure will not present any of the critical layer-to-layer or first turn to last turn contribution due to the fact that the increased fill factor will allow implementing the same amount of turns in a single layer structure with a large gap between first and last turn. Moreover, this structure presents a reduced turn to core capacitance contribution respect to the conventional windings because of the reduced A/d ratio. To finalize the comparison, as suggested in [14], the effect of adding a small inductor with very low capacitance in series with a multilayer high capacitance design is analyzed by constructing two single layer toroids using one core and three stacked cores Magnetics® Kool Mμ 125 0077350A7 with an inductance value of 25.9 and 69.9 μH respectively. The implemented prototypes are presented in Fig. 2 and the impedance measurements results are shown in Fig. 3 and Fig. 4.

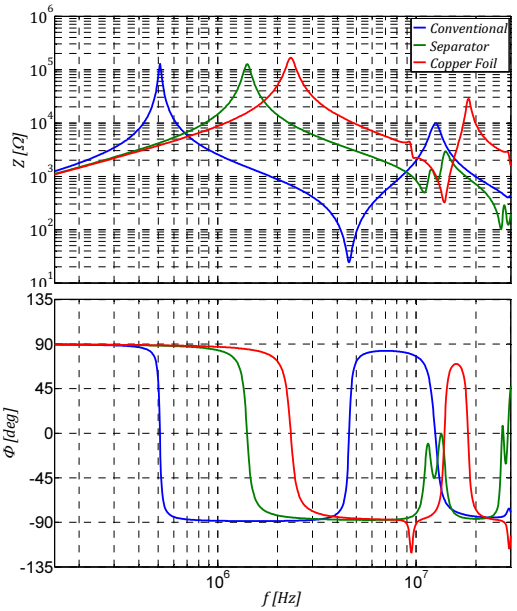

Fig. 3. Impedance and phase magnitudes in the conducted EMI frequency range ($150\ kHz - 30MHz$) for the conventional (blue), separator (green) and copper foil (red) inductors.

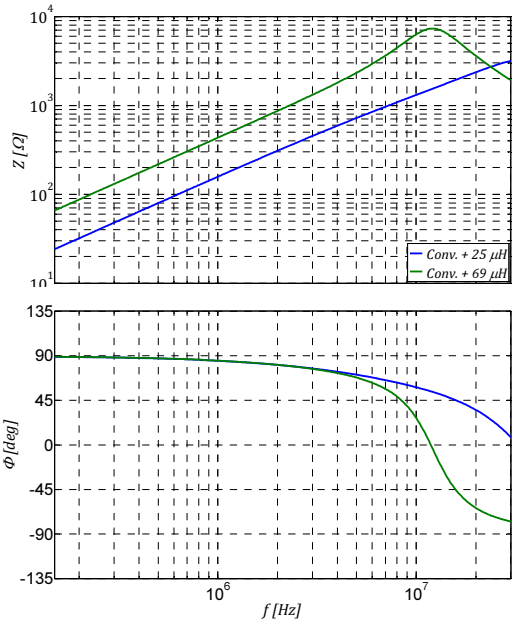

Fig. 4. Impedance and phase magnitudes in the conducted EMI frequency range ($150\ kHz - 30MHz$) for the small size inductors 25 μH (blue), 69 μH (green).

The parallel capacitance is calculated from the measured parallel resonant frequency and inductance value. The obtained values are shown in Table I.

TABLE I
PROTOTYPES' INDUCTANCE AND CAPACITANCE VALUES

Prototype	$L\ [mH]$	$f_0\ [MHz]$	$C_p\ [pF]$
Conventional	1.21	0.51	80.5
Separator	1.16	1.41	11
Copper Foil	1.15	2.34	4
25 μH	0.0259	32.5	1
69 μH	0.0698	11.8	2.7

As it can be observed form Table I, the two layer structure with separator has seven times lower capacitance than the conventional structure due to the reduced layer to layer capacitance and the inserted gap between the first and last turn in each of the layers. The copper foil implementation reaches a capacitance level twenty times lower than the conventional structure. Even with a much larger turn to turn capacitance this structure achieves the smallest parasitic capacitance value. Finally, the low size implemented inductors present a quasi-ideal behavior up to 30 MHz with a parasitic capacitance of 1 and 2.7 pF respectively.

IV. CONDUCTED EMI MEASUREMENTS

The EMI performance of the different implemented prototypes is analyzed using an ac-dc converter evaluation board from Texas Instruments PMP669 (Fig. 5) where the dc-dc conversion power stage has been disabled and the input EMI filter completely removed.

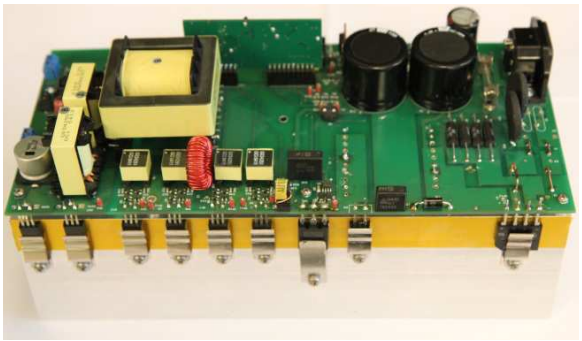

Fig. 5. AC-DC converter with conventional PFC. Evaluation board from Texas Instruments PMP669 MB

The EMI measurement is performed using a Two-line V-Network (LISN) with the converter operating @ $f_{sw} = 98\ kHz$ $V_{ac} = 230\ V_{rms}$ and $P_o = 200\ W$. Fig. 6 shows the measurement result for the three main different prototypes. Fig. 7 shows the effect of adding the small inductor in series with the conventional two layer inductor.

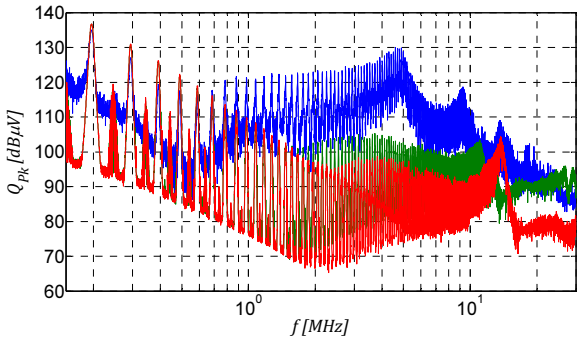

Fig. 6. EMI measurement using LISN network from 150 kHz to 30 MHz @ 230 V_{rms} and 200 W for the conventional (blue), separator (green) and copper foil (red) implemented inductors.

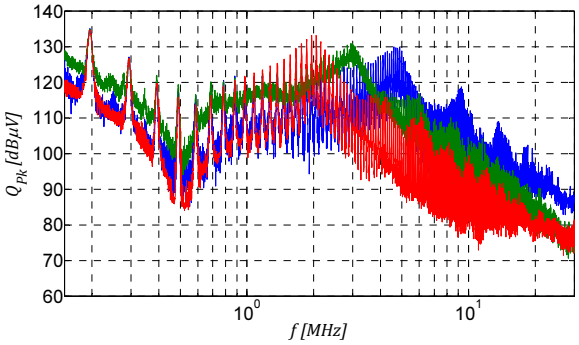

Fig. 7. EMI measurement using LISN network from 150 kHz to 30 MHz @ 230 V_{rms} and 200 W .Conventional (blue), conventional+ 25 μH (green), and conventional+ 68 μH (red).

The capacitance reduction obtained in the two layers with separator and the copper foil implementations provide a significant reduction in conducted EMI ss it can be observed in Fig. 6. The conventional structure shows high amplitude harmonics around 5.5 MHz which corresponds to the location of the minimum impedance measured for this prototype (Fig. 3). Fig. 7 shows the small effect of adding a small series inductance in series with the conventional two layer inductor. In fact, as it can be observed, the high frequency noise will be reduced due to the increased impedance in this area. On the other hand, at low frequencies, the introduction of this inductance will reduce the frequency of the minimum inductor impedance, increasing the propagated noise due to the higher amplitude of the switching frequency harmonics and the increased quality factor at this resonant frequency due to the reduced ac resistance.

V. EVALUATION OF THE IMPACT ON THE SWITCHING AND CONDUCTION LOSS

After comparing the different configurations in terms of conducted EMI, an efficiency related comparison is performed using a low inductive double pulse tester (DPT) shown in Fig. 8. A small die size 600V super-junction device FCD9N60N from Fairchild Semiconductor is used in combination with a 600V SiC diode IDD10SSG60C from Infineon Technologies.

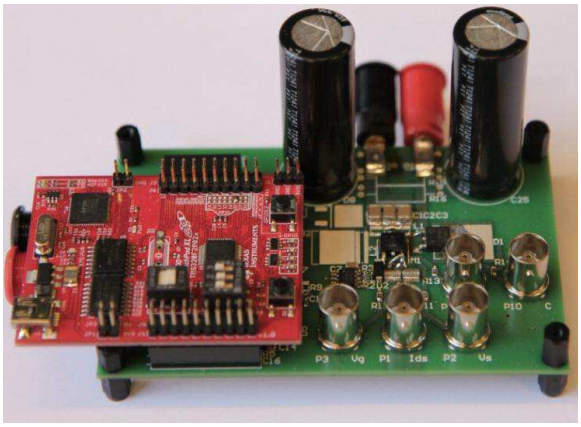

Fig. 8. Implemented double pulse tester prototype.

Fig. 9 shows the DPT switching waveforms for the conventional inductor (green current) and the copper foil prototypes for an inductor current level of 6A and a bus voltage of 400V. Fig. 10 shows the switching waveforms for the conventional two layer inductor (green current) in series with the 25 μH (purple) and the 69 μH (blue) prototypes.

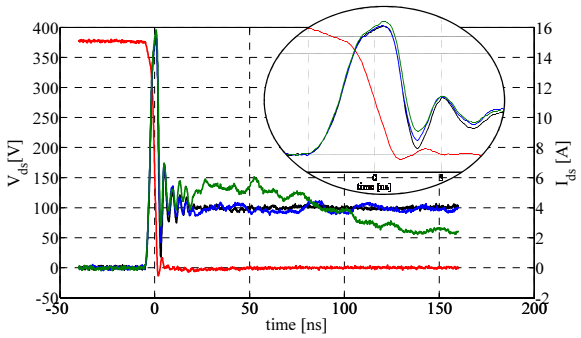

Fig. 9. Switching waveform comparison between the conventional (green current waveform) and the copper foil (blue current waveform) inductor prototypes.

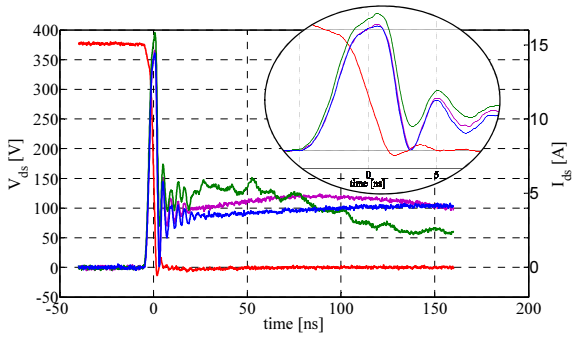

Fig. 10. Switching waveform comparison between the conventional (green current waveform) and conventional with series 25 μH (purple) and 69 μH (blue) inductor prototypes.

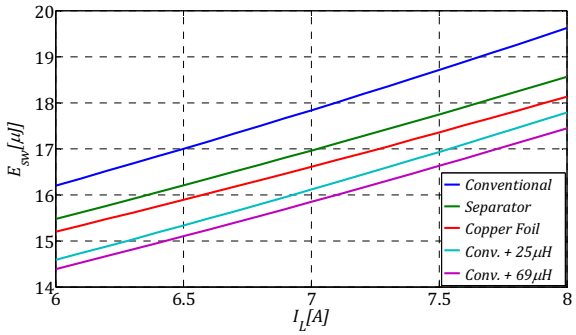

Fig. 11. MOSFET switching energy as a function of the inductor current level for the different inductor prototypes.

After performing a switching energy loss extraction, the turn on energy dissipated in the MOSFET is plotted as a function of the inductor current level (Fig. 11). As it can be observed, a small difference is obtained in the MOSFET turn on loss due to the inductor parasitic capacitance effect. Acording to the difference in calculated capacitance value and according to (2), the difference in energy loss from the standard double layer and the copper foil inductors should be at least 6 μJ

$$E = \frac{1}{2} \cdot C \cdot V^2 \qquad (2)$$

However, this difference from the measurement to the calculation can be easily explained by looking at Fig. 9 and Fig. 10. As it can be observed the dissipated energy in the MOSFET before the drain to source voltage collapses to zero varies very little between the different measurements. This is due to the fact that the parasitic capacitance will not be charged on this small subinterval. Instead this capacitance will resonate with the parasitic inductance formed by the inductor interconnection and will finalize the charge long time after the switch has completed the switching transition. It can be concluded that the charge of the parasitic capacitance will not create a large increment in the MOSFET switching loss but it will increase the conduction losses in the inductor because of the presence of a high frequency resonant current that will be damped by the component ac resistance. Furthermore, there is also a risk that these resonances can couple through parasitic capacitances to the converter structure and generate common mode noise source further challenging the input EMI filter. Finally, as it can be observed in Fig. 10 the inclusion of the small size inductors in series with the standard double layer inductor will effectively reduce the frequency of this resonance minimizing the joule losses in the circuit because of the reduced ac resistance effect at lower frequencies.

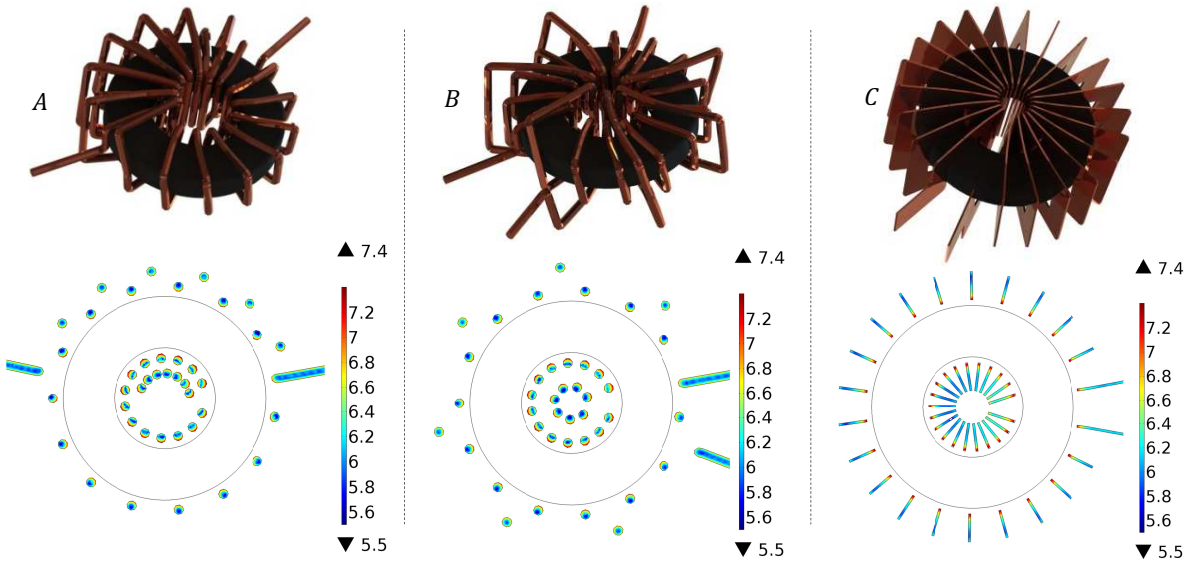

Fig. 12. Simulated inductor structures and 2d plots of the windings current density. A-Conventional double layer, B-Double layer with separator, C-Copper foil.

In order to complete the analysis of the different designs is important to evaluate the ac resistance of the different structures. This is a very important parameter in PFC applications with boundary conduction mode (BCM) operation where the inductor current presents a large high frequency component. Ac resistance measurement of inductors is a difficult task because when the measurement is performed, the magnetic material losses are included in the measurement and they are difficult to separate from each other. Another possibility is to perform an analytical calculation based on Dowell equations (3) where h is the copper thickness amd δ is the skin depth.

$$\frac{R_{ac,m}}{R_{dc,m}} = \frac{\xi}{2}\left[\frac{\sinh\xi + \sin\xi}{\cosh\xi - \cos\xi} + (2m-1)^2\frac{\sinh\xi - \sin\xi}{\cosh\xi + \cos\xi}\right]$$

$$\xi = \frac{h}{\delta} \qquad \delta = \frac{7.5}{\sqrt{f}} \quad [cm] \qquad (3)$$

However even considering that this work takes into account skin and proximity effects, it will not provide a correct solution in this specific problem where a 3d structure is evaluated with a variable distance between turns and layers. Instead, a finite element analysis (FEA) is performed by constructing a 3d model of the different analyzed winding strategies. The size of the simulated inductors is reduced to minimize the complexity of the solution. The same copper cross section $A = 0.56\,mm^2$ is used in the simulated structures. The three implemented models are shown in Fig. 12. A simulation is performed where the ac resistance is calculated for different frequencies up to 400 kHz. The windings are meshed to take into account the skin effect. Fig. 12 shows a current density plot of the three different structures at a frequency of 400 kHz represented with a logarithmic colorbar. The skin effect can be easily appreciated in the inductor terminals in the conventional and the separator structures. All the structures present a higher current density near the core due to the high concentration of flux lines in the core proximity. The proximity effect of the second layer can be seen in the inner part of the toroid in the conventional structure where the first layer presents a high current density area in the close proximity to the second layer windings.

The obtained ac resistance for the different structures is shown in Fig. 13. All the structures present a similar ac resistance value at 100 Hz of around 18 $m\Omega$. The conventional structure ac resistance value increases up to 1.54 Ω compared with 1.07 Ω and 0.63 Ω for the separator and copper foil structures respectively.

Finally, the effect of the parasitic capacitance in the converter efficiency is analyzed by testing the copper foil and the conventional implemented inductor prototypes in a PFC stage operating in BCM. The power stage is a modular PFC design operated with a superjunction 600V MOSFET 65R230C7 and a SiC 600V diode IDD04SG60C. The MOSFET is driven by a high current 9A driver FAN3122 and controlled by a BCM controller FAN7930B. Fig. 14 shows the implemented PFC power stage and Fig. 15 shows the measured converter efficiency as a function of the converter output power for a constant dc input voltage $V_{in} = 200V$ and an output voltage $V_{out} = 375V$.

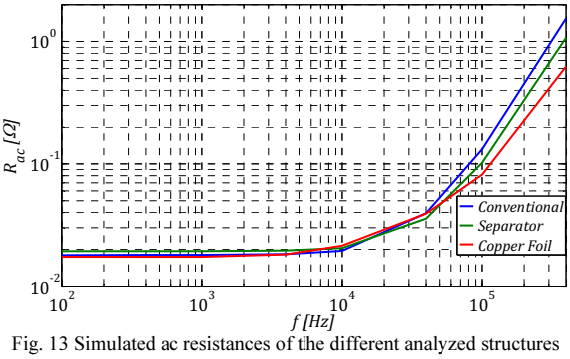

Fig. 13 Simulated ac resistances of the different analyzed structures

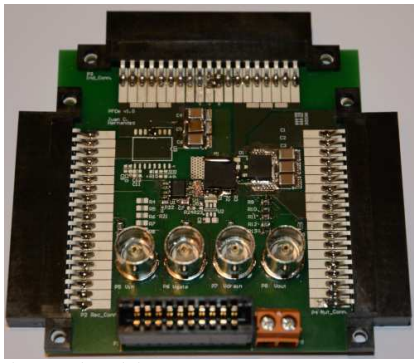

Fig. 14 Implemented modular PFC power stage

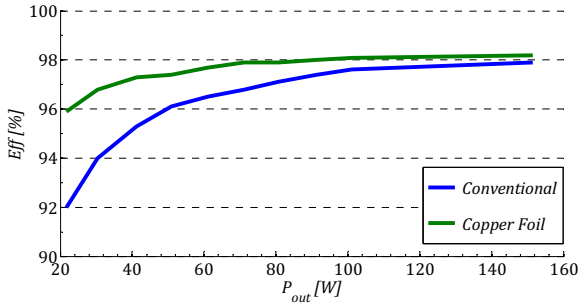

Fig. 15 Measured efficiency as a function of the converter output power for $V_{in} = 200\,V$ and $V_{out} = 375\,V$.

The effect of the capacitance can be appreciated at very low power levels. Under this situation, the converter switching frequency is increased up to $215\,kHz$. The difference in power loss between the two solutions is $0.96W$. With the operating voltage levels, the inductor parasitic capacitor changes its voltage from $200V$ to $-175V$. Taking into account the measured capacitance for the two prototypes, this change in voltage corresponds to a dissipated energy difference of $2.7148\,\mu J$ which corresponds to a power loss difference of $0.58\,W$. Therefore the remaining power loss difference is attributed to ac resistance difference between the two structures. As it can be seen, as the converter output power increases the two efficiency measurements get closer because the converter switching frequency is reduced down to $48\,kHz$ at $150\,W$ output power, minimizing the ac resistance difference between the prototypes.

VI. Conclusions

This paper analyzes different inductor winding structures focusing on parasitic capacitance reduction of the component. The parasitic capacitance effects are analyzed from conducted EMI and efficiency point of views. Different solutions for reduced capacitance effects are evaluated. The ac resistance of the different structures is evaluated together with the capacitance because it has a large impact on PFC converters efficiency operating in BCM mode. A copper foil winding structure is proposed with very low parasitic capacitance and ac resistance compared to the conventional structures. This foil winding structure is similar to using PCB windings in a U core or E core structure. Using a single layer configuration can be very effective in reducing the parasitic capacitance mitigating EMI conducted and radiated problems and improving the converter efficiency. Moreover high frequency PFC converters operating in BCM will benefit from a reduced winding ac resistance

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Evaluation of 600V Superjunction Devices in Single Phase PFC Applications under CCM Operation

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Evaluation of 600V Superjunction Devices in Single Phase PFC Applications under CCM Operation

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***Abstract*— This paper presents a power density/efficiency evaluation in single phase power factor correction (PFC) applications operating in continuous conduction mode (CCM). The comparison is based on semiconductor dynamic characterization and a mathematical model for prediction of the conducted electromagnetic interference (EMI). The dynamic characterization is based on a low inductive double pulse tester (DPT). The measured switching energy is used in order to evaluate the devices performance in a conventional PFC. This data is used together with the mathematical model for prediction of the conducted electromagnetic interference. The method allows comparing different devices and evaluating the performance as a function of the PFC power density and efficiency.**

Keywords*— Power factor correction, continuous conduction mode, EMI prediction.

I. INTRODUCTION

Power factor correction circuits are widely use in industrial and household applications to fulfill the power factor and harmonic standards. These types of circuits are traditionally used in continuous conduction mode configuration [1], [2]. This operation mode presents lower component current stress than critical or boundary conduction modes (BCM) which are actually preferred for low power levels because of their control simplicity [3]. The main disadvantage of continuous conduction mode PFC is the rectifier reverse recovery loss [2] which limits the converter operating switching frequency and consequently its power density. However, the latest achievements in semiconductor technology including the adoption of wide bandgap semiconductor materials makes it possible to eliminate this reverse recovery problem [4], [5], [6] allowing higher converter operating switching frequencies. Moreover, the recently introduced wide bandgap gallium nitride (GaN) transistors with a higher electrical field strength and electron mobility than Si based switches [7] makes it possible to reduce the device die size decreasing the parasitic capacitances. This reduction of die size enables higher operating switching frequencies to further increase the converter power density while reducing the cost without deteriorating the efficiency. This paper presents a design oriented methodology for power factor corrector implementation based on double pulse tester (DPT) dynamic characterization and a conducted EMI prediction model. In this way it is possible to evaluate the switch-diode pair energy loss across half a line cycle. At the same time, the inductor size can be estimated based on the maximum energy storage requirement $E = 1 / 2 \cdot I_{peak}^2 \cdot L$. The input filter requirement can be evaluated based on the calculated quasi peak and average noise from the calculated harmonics across half the line cycle. This work performs an evaluation of state of the art 600V superjunction silicon (Si) devices in combination with silicon carbide rectifiers (SiC). The devices performance is evaluated for various input inductor values and switching frequencies.

II. DYNAMIC CHARACTERIZATION

The evaluation of the semiconductors switching behavior can be performed based on analytical models [8], [9], [10]. However, this is an arduous work that is technology dependent. In this work, the devices dynamic characterization is performed in a low inductive DPT. This circuit is the basic configuration used to evaluate the dynamic performance of different semiconductor technologies under clamped inductive load operation. The basic schematic is presented in Fig.1. The typical operating waveforms of the DPT are shown in Fig. 1. At the time interval t_0 the MOSFET is turned and the inductor current increases up to the desired current level. Once the desired level is reached, the MOSFET is turned off at t_1. At t_2 and t_3 the MOSFET is turned on and turned off again and the associated energy loss is measured for the desired current level.

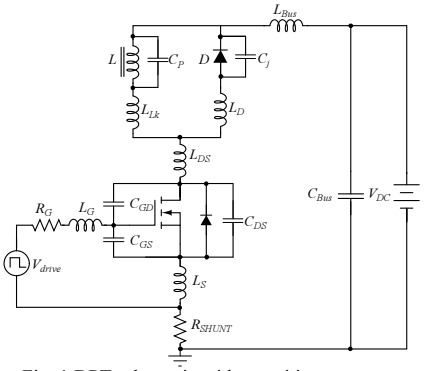

Fig. 1 DPT schematic with parasitic components

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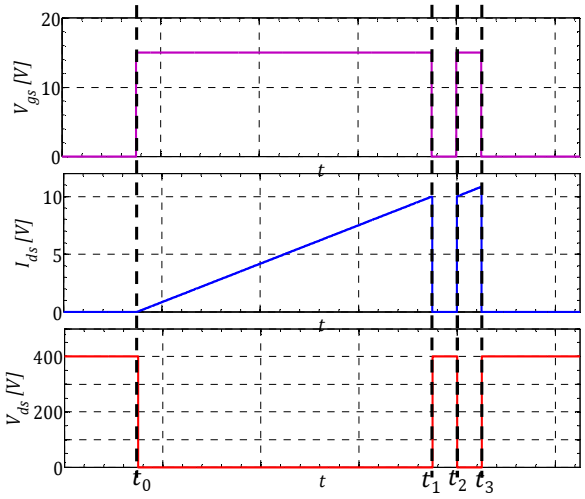

Fig. 2 DPT typical operating wavefoms

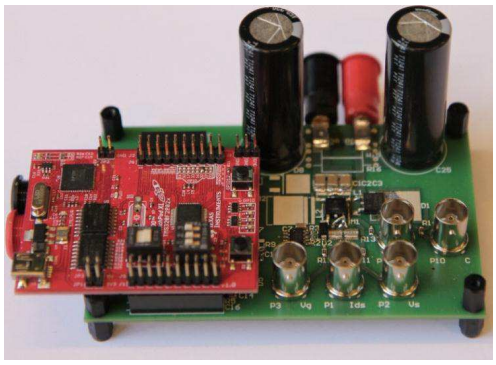

Fig. 3 DPT Experimental prototype

In order to perform the semiconductors characterization, a DPT prototype has been designed paying special attention to minimize the parasitic inductances and capacitances in the switching loop [11], [12] [13]. The main switch current is measured using a flat current shunt structure as presented in [14] to minimize the parasitic inductance inserted in the loop and maximize the current measurement bandwidth. The implemented prototype (Fig. 3) is based on the a DSP evaluation board Piccolo Launchpad XL and can accommodate both Dpak and PQFN packages for the main switch and the diode.

III. Conducted EMI Prediction Model

A conducted EMI estimation is necessary to evaluate the input filter requirement of the converter. The level of attenuation required according to the standards will determine the input filter corner frequency and consequently its volume. The analyzed topology in this work, is the conventional boost derived PFC rectifier shown in Fig. 4. The input inductor current waveforms can be derived by looking at the volt/second balance across the component as shown in Fig. 5. The MOSFET M on time D_1 can be calculated according to [15] as presented in (1) for continuous conduction mode and (2) for discontinuous conduction mode, where $M = V_o/V_{in}$ and $K = 2L_{IN} \cdot T_S/R_L$. The transition from discontinuous to continuous conduction mode the two modes can be estimated by evaluating the input current condition $I_{in} \leq D_{cont}T_S V_{IN}/2L_{IN}$. The diode D conduction time can be calculated as $D_2 = 1 - D_{cont}$ for continuous and $D_2 = K \cdot M/D_{dis.}$ for discontinuous conduction modes. If the input current is sampled at different points in time, is possible to calculate the inductor current using piecewise linear definition as shown in Fig. 6. Then, by using (3) the inductor current frequency harmonic content at each time interval is calculated.

$$D_{cont} = (M-1)/M \cdot \tag{1}$$

$$D_{discont} = \sqrt{K \cdot M \cdot (M-1)} \cdot \tag{2}$$

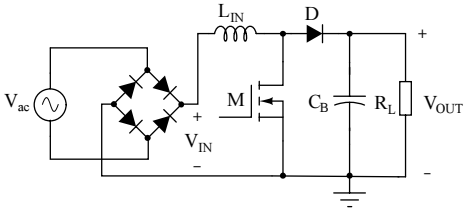

Fig. 4 Conventional single phase PFC circuit

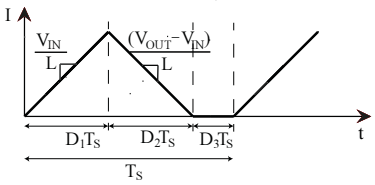

Fig. 5 Inductor current waveform

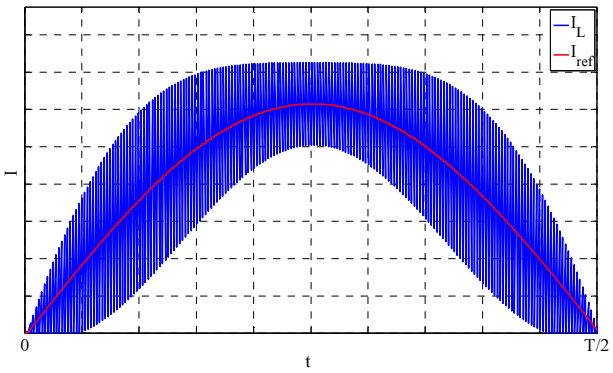

Fig. 6 Calculated inductor current following the current reference through half line cyle

$$I_L(t) = a_0/2 + \sum_{n=1}^{N}(a_n \cos(2\pi nt/T_s) + b_n \sin(2\pi nt/T_s)) \tag{3}$$

Once the inductor current harmonics have been calculated it is possible to estimate the EMI receiver quasi-peak and average readings. As shown in Fig. , the inductor current harmonics are first multiplied by the LISN network differential gain which can by approximated by (4) where the equivalent impedance Z_C is calculated as $Z_C = Z_B \| (1/sC_3 + R_3)$ where $Z_B = (sL_1 + 1/sC_1 + R_1) \| (1/sC_2 + R_2) + sL_2$.

$$G_{LISN}(f) = \frac{V_A}{I_L} = \frac{Z_c}{R_3 + 1/sC_3} \cdot R_3 \quad (4)$$

Then, the EMI receiver sweeps the frequency range of interest by using a near Gaussian filter which transfer function can be approximated as (5) as presented in [3]. The envelope detector will detect the harmonic peak value through half line cycle from which the average and the quasi peak values can be extracted. However, the quasi-peak value is based on a quasi-peak detector which transfer function is nonlinear. The output of this quasi-peak detector can be calculated as shown in [3]. By using a dissection method like a dichotomy algorithm or method of division in halves applied over the charge balance on the capacitor (6) were the discharge resistance is known to be 160 times the charge resistance value.

$$G_{IF}(f, f_{IF}) = e^{-(f-f_{IF})^2/c^2} \text{where } c = 4.5e^3/\sqrt{ln2} \quad (5)$$

$$\sum_1^n \int_{a_n}^{b_n} \frac{V_{envelope} - V_{quasi}}{1} = \int_0^{T_s/2} \frac{V_{quasi}}{160} - \sum_1^n \int_{a_n}^{b_n} \frac{V_{quasi}}{160} \quad (6)$$

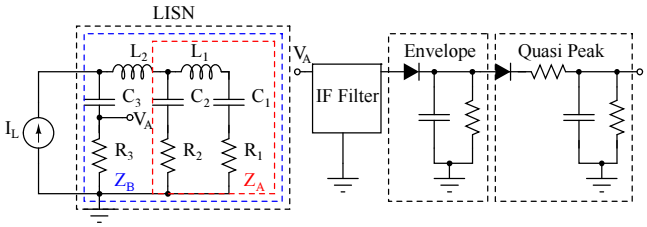

Fig. 7 LISN network, envelope and quasi peak detector schematics

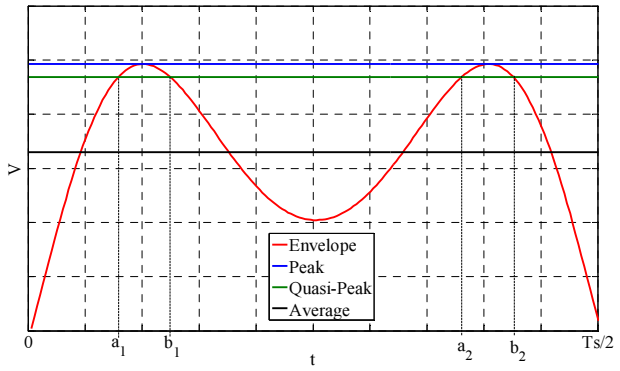

Fig. 8 Envelope, peak, quasi peak and average signals for the inductor current first harmonic across half line cycle

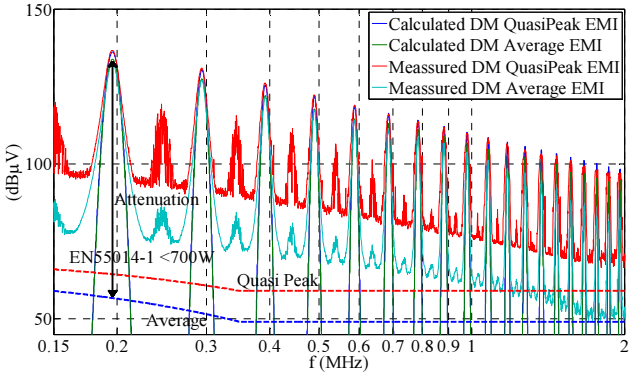

Fig. 9 Calculated vs. measured quasi peak and average conducted EMI

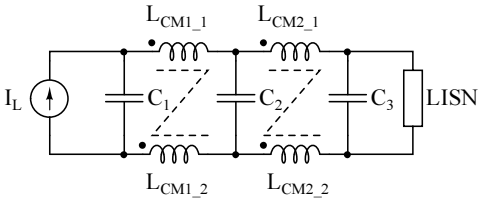

Fig. 10 Two stage pi filter loaded with the lisn network

The quasi peak value is calculated finding the charge balance condition in the capacitor by integrating the capacitor charge and discharge currents across half line cycle. In the same way, the peak value will be the envelope absolute maximum value, and the average is obtained by averaging the envelope through half line cycle as shown in Fig. 8. Fig. 9 presents the calculated and the measured quasi peak and average values for a CCM PFC operating at $V_{IN} = 230V_{rms}$ and $V_{OUT} = 386V$ with an inductance value $L_{IN} = 1150\,\mu H$ and an output power level $P_{OUT} = 200W$. After obtaining the calculated converter EMI quasi peak and average values, is possible to calculate the necessary amount of attenuation required to fulfill the limits established by the standard. In this work, a two stage π filter (Fig. 10) is selected for the evaluation. This type of filter with attenuation equal to 100dB/dec will set the necessary filter corner frequency for the necessary amount of attenuation required.

IV. EVALUATION

In this section, two state of the art superjunction devices with three SiC rectifiers are evaluated for a PFC application under the following conditions: $V_{IN} = 230V_{rms}$, $V_{OUT} = 400V$ and $P_{OUT} = 200W$ The selected superjunction devices have $130m\Omega$ and $230m\Omega$ on resistances, and the SiC diodes have a continuous forward current capability of 6, 8 and 10 A. As it can be observed in Fig. 11, the diode selection does not modify the MOSFET turn off loss. At zero current level, the amount of measured energy will be equal to the stored energy in the MOSFET output capacitance that will be dissipated at the MOSFET turn on. In this case, the device with the larger die presents a higher turn off loss. According to Fig. 12 both MOSFET present a very similar turn on loss. As it can be seen, at the turn on the energy stored in the diode output capacitance will create a current level independent turn on loss.

By performing an interpolation on the obtained characterization data, the semiconductor switching losses can be obtained through half line cycle and averaged to calculate the total semiconductor switching loss. In the same way, the semiconductor conduction loss is calculated (7) by using the manufacturer MOSFET on resistance (R_{DS}) and by extracting the diode threshold voltage (V_T) and dynamic resistance (R_D) from the characteristic I-V curve.

$$P_{cond.} = I_{M,rms}^2 \cdot R_{DS} + I_{D,avg} \cdot V_T + I_{D,rms}^2 \cdot R_D \quad (1)$$

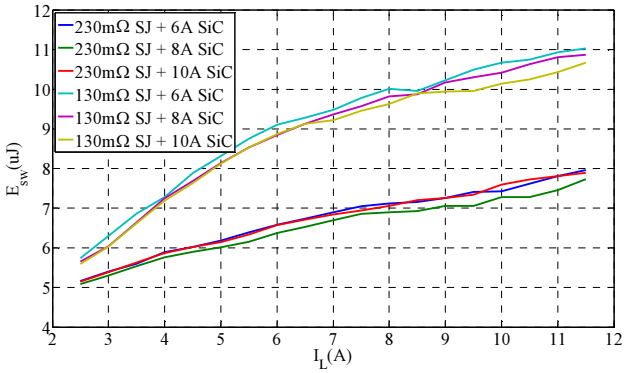

Fig. 11 DPT turn off energy loss as a function of the inductor current level

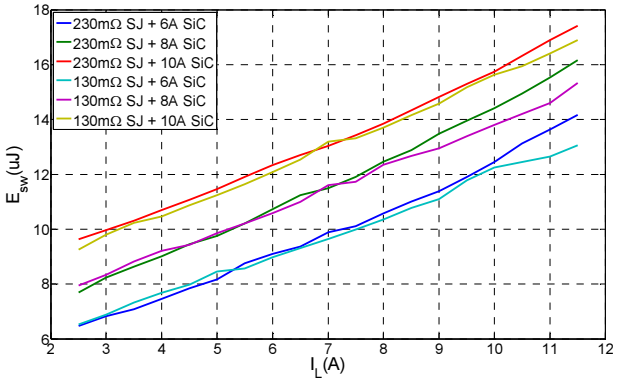

Fig. 12 DPT turn on energy loss as a function of the inductor current level

The total semiconductor efficiency loss can be plotted then as a function of the converter switching frequency for different input inductor values as shown in Fig. 13. At low frequency values, the semiconductor loss will be increased because the semiconductor current stress will be increased by increasing the inductor ripple current and the time the converter operates in discontinuous conduction mode (DCM) through the line cycle. As the converter switching frequency increases, the semiconductor switching loss is increased but the conduction loss is decreased creating a semiconductor minimum loss for each inductor value. The inductor current stress ($I_{L,rms}^2$) can be plotted to obtain a figure of the inductor winding losses

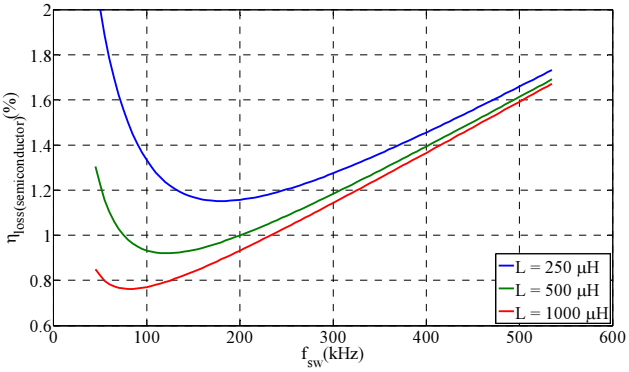

Fig. 13 Semiconductor total efficiency loss (130 mΩ superjunction MOSFET + 6A SiC diode) as a function of the converter switching frequency

Fig.14 shows how the stress diminishes as a function of the converter frequency and inductance value. However, this is not a valid measure for comparison because the inductor winding resistance will change as a function of the inductance value and the energy storage requirement. Fig. 15 shows the maximum calculated inductor energy storage requirement ($I_{L,peak\_max}^2/2L$). As it can be observed, as in the current stress case, the value decreases as the switching frequency increases reaching an absolute minimum as the inductor ripple approaches zero.

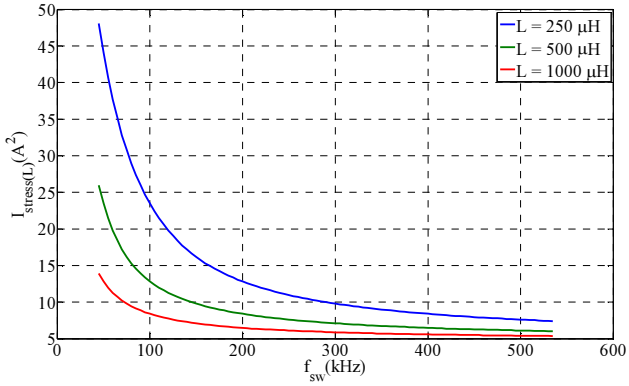

Fig. 14 Inductor current stress as a function of the converter switching frequency

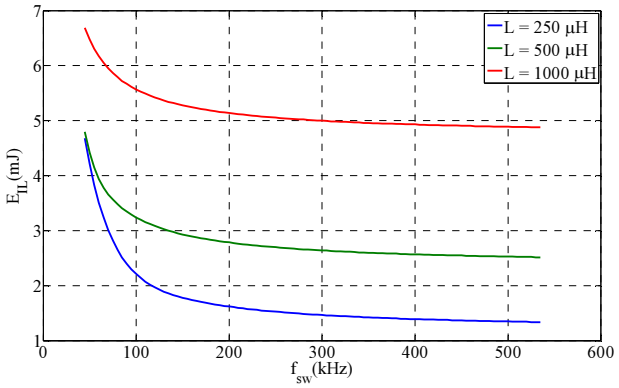

Fig. 15 Inductor energy storage requirement as a function of the converter switching frequency

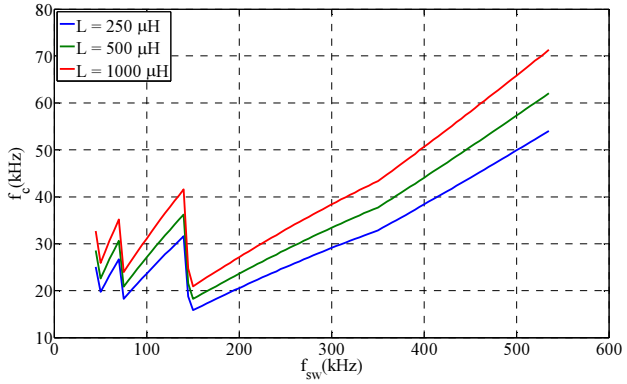

Fig. 16 Input filter corner frequency as a function of the converter swiching frequency

Fig. 16 presents the input filter corner frequency requirement. Obviously, the volume of this filter is affected by the input inductor ripple, and consequently its energy storage requirement. Therefore the only viable way of increasing the converter power density, is by increasing the converter switching frequency. The filter corner frequency presents local minimum values at 50, 75 and 150 kHz due to the 150 kHz limit of the standard. When the converter operating switching frequency approaches these frequencies, the third, second and first harmonic of the converter operating switching frequency hit the measurement frequency range increasing the input filter attenuation requirement. This is the reason why a common practice in industry is to design converters operating just below these frequency levels to limit the switching loss while minimizing the input filter volume.

Fig. 17, 18 and 19 show the calculated semiconductor loss for the $130m\Omega$ MOSFET with the $10A$ diode and the $230m\Omega$ MOSFET with the 6 and $10A$ diodes respectively. As it can be observed, the smaller superjunction device performs better than the $130m\Omega$ version at switching frequencies higher than 150 kHz due to the smaller turn off loss. It is only at very low frequency and for the large inductance value, when the lower channel resistance of the $130m\Omega$ device offers a small advantage over the smaller device. The predominant conduction losses correspond to the diode. This can be observed by the fact that even considering the increased turn on loss, when a larger diode is used, the efficiency loss is increased for the whole frequency range evaluated.

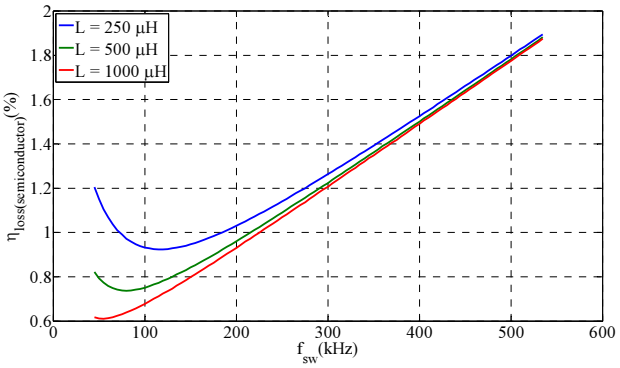

Fig. 17 Semiconductor total efficiency loss (130 mΩ superjunction MOSFET + 10A SiC diode) as a function of the converter switching frequency

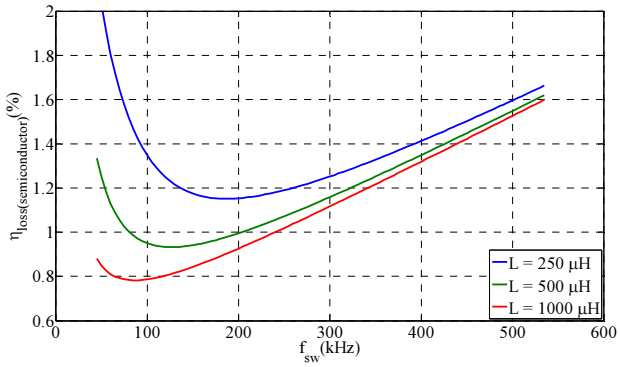

Fig. 18 Semiconductor total efficiency loss (230 mΩ superjunction MOSFET + 6A SiC diode) as a function of the converter switching frequency

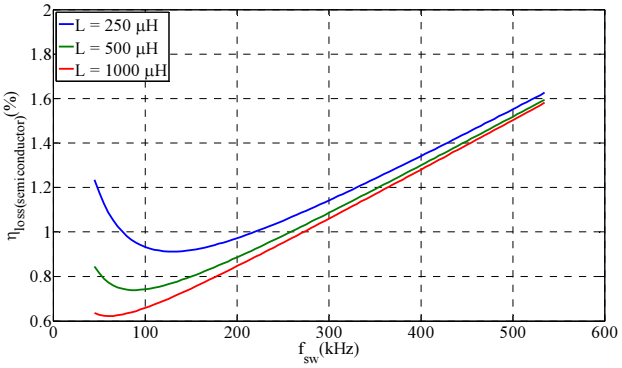

Fig. 19 Semiconductor total efficiency loss (230 mΩ superjunction MOSFET + 10A SiC diode) as a function of the converter switching frequency

If we compare the different evaluated devices, the larger MOSFET and diode with the large inductor at $45\ kHz$ would give the best performance in terms of efficiency with only 0.62% efficiency loss due to semiconductor conduction and switching loss. The necessary input filter corner frequency is situated at $32.6\ kHz$, and the calculated inductor energy storage requirement is $6.7\ mJ$. If the switching frequency is now increased up to the next local maxima in the input filter corner frequency ($@\ 70\ kHz$), the best performance is obtained from the $230m\Omega$ device with the $10A$ diode and maximum inductance value. With only 0.63% total semiconductor loss this would be the correct choice even when the efficiency is the maximum priority. This solution would increase the filter corner frequency 8% and reduce the input inductor energy storage requirement by 12% without having a negative impact on the semiconductor loss. If the $500\ \mu H$ inductor is selected at this operating frequency, the input inductor size could be reduced down to 46.7% the volume of the initial design $@\ 45\ kHz$. This selection would increase semiconductor losses by 20% and lower the input filter corner frequency by 6% respect to the initial design. If we move now towards the next maxima in the input filter corner frequency, the obvious selection is the mid-size inductor with the small MOSFET and the large diode. At this operating frequency, the input inductor energy requirement is reduced 55.5% and the input filter corner frequency is increased by 11% while the semiconductor loss is increased 27% respect to the original design. This power loss increase could be alarming, but the semiconductor power loss is still only 0.79% of the converter output power. If the design needs to be optimized for power density, the small inductor size could be chosen at a switching frequency of $350\ kHz$. This selection would give the same requirement in input filter corner frequency than the initial design with an inductor energy storage requirement reduction of 79% with a total semiconductor loss 2 times larger respect to the initial design.

V. CONCLUSIONS

This paper presents a comprehensive design/evaluation procedure for single phase PFC applications. The method is based on a mathematical model for prediction of the conducted differential mode EMI and a semiconductor dynamic characterization setup. The proposed method evaluates the input filter corner frequency requirement and the input inductor

energy storage requirement to compare different solutions in terms of power density. The obtained characterization data allows predicting the semiconductor switching loss in a precise way making possible to compare the different evaluated devices under different operating conditions. A case design is presented where two superjunction devices are analyzed together with three SiC diodes to evaluate several possible solutions regarding converter efficiency and power density. As it can be observed, limiting the converter switching frequency in the way that only the second or the third harmonic need to be attenuated is not the best solution in terms of power density. As observed in Fig. 20, as the semiconductors switching speeds increase is possible to operate beyond the 150 kHz filter corner frequency maxima achieving a high volume reduction of the input inductor size without penalizing in the input filter size and with a small penalty in terms of semiconductor loss. Solution 1 operates at $45\,kHz$ while solution 2 operates at $350\,kHz$ with more than 5 times input inductor size reduction and with a MOSFET die size 56% times the size employed in the first solution. With the same filter corner frequency the semiconductor power loss penalty is only 3.15 W for a converter output power of 500W (0.63% efficiency loss respect to solution 1). With the new introduced GaN switches this tendency will be accentuated making possible to increase the converter power densities with very small efficiency penalties.

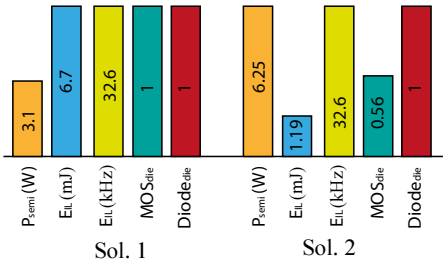

Fig. 20 Two opposite solutions in terms of efficiency vs power density. Sol. 1: 130mΩ MOSFET with the 10Adiode @ 45 kHz and Sol. 2: 230mΩ MOSFET with the 10Adiode @ 350 kHz

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Characterization and Evaluation of 600 V Devices for Active Power Factor Correction in Boundary and Continuous Conduction Modes

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Characterization and Evaluation of 600 V Range Devices for Active Power Factor Correction in Boundary and Continuous Conduction Modes

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***Abstract*—Traditional characterization of semiconductors switching dynamics is performed based on clamped inductive load measurements using the double pulse tester (DPT) configuration. This approach is valid for converters operating in continuous conduction mode (CCM), however in boundary conduction mode (BCM), if valley switching detection is used, the amount of energy recovered from the semiconductor output capacitance and the converter switching frequency need to be accurately calculated. This paper presents a characterization and evaluation procedure for conventional power factor correction circuits operating in CCM and BCM.**

Keywords—Power Factor Correction; Continuous; Boundary; Characterization; Evaluation.

I. INTRODUCTION

New semiconductor technologies, has made traditional converter operation modes to become obsolete for high switching frequency/high power density converters design. Traditional active power factor correction (PFC) circuits are based on a conventional boost converter, where the average input inductor current is controlled to achieve close to unity power factor. In high power applications continuous conduction mode (CCM) is the most used operation mode because of the reduced current stress. However, at lower power levels boundary conduction mode (BCM) is often preferred due to its low control complexity, not requiring converter input current sensing. The MOSFET on time is kept constant over the grid line period achieving an inherent proportionality between the converter input voltage and input current [1]. Power factor correction converters operating in BCM operate at the boundary between continuous and discontinuous conduction mode (DCM) [1], [2].producing the converter switching frequency to vary across the line cycle. This operation mode allows increasing the converter switching frequency due to the reduced switching losses with zero current switching (ZCS) operation at turn on. Moreover, zero voltage switching (ZVS) can also be achieved if a valley switching detection control scheme is used. The aim of this work is to compare state-of-the-art 600 V range devices performance by following a characterization procedure that can be used for both CCM and BCM. This paper presents a comparison and evaluation method based on a model for accurate prediction of the converter switching waveforms with special focus on the switching frequency prediction during BCM operation.

II. CHARACTERIZATION AND EVALUATION PROCEDURE

The characterization procedure is based on a double pulse tester (DPT) measurement. This circuit is the traditional clamped inductive load test set-up shown in Fig. 1. The device under test (DUT) is evaluated by building up some current in the inductor L, by keeping the device on for a controlled amount of time. When the required current level across the inductor has been reached, the DUT is turned off and on again, and the switching energy can be evaluated by integrating the V_{DS} times I_{DS} of the device. By repeating this procedure for different current levels, it is possible to create a set of data containing the switch-diode pair energy loss as a function of the current level.

In order to evaluate the performance of the evaluated devices, in this work a conventional boost based active power factor correction circuit as shown in Fig. 2 has been used. When the converter operates in CCM, the converter inner current loop adjusts the MOSFET on time to achieve unity power factor. Most of the time the inductor current is in CCM, however, as the converter approaches the zero crossings of the rectified input voltage waveform, the inductor current enters DCM operation. The necessary MOSFET on time can be calculated [3] as presented in (1) and (2) for CCM for DCM operation, respectively. The parameter M is defined as the dc voltage ratio as shown in (3), where V_{in} is the instantaneous converter input voltage. The value K is calculated as shown in (4). The

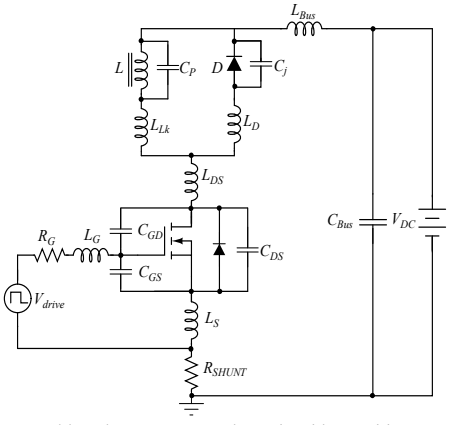

Fig. 1. Double pulse tester DPT schematic with parasitic components

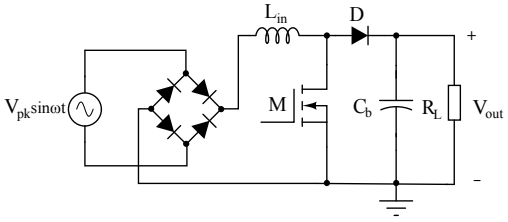

Fig. 2. Boost single phase PFC converter schematic

transition between CCM and DCM can be found as in (5). Finally, the inductor discharge interval can be found as presented in (6) and (7) for continuous and discontinuous conduction modes, respectively. Fig 3 shows the piecewise linear inductor current definition for discontinuous conduction mode. By using this definition, it is possible to find the converter currents across a half line cycle to calculate the semiconductor conduction losses, and interpolate the switching losses from the obtained DPT characterization data.

$$D_{CCM} = \frac{(M-1)}{M} \tag{1}$$

$$D_{DCM} = \sqrt{K \cdot M \cdot (M-1)} \tag{2}$$

$$M = \frac{V_{out}}{V_{in}} \tag{3}$$

$$K = \frac{2L_{in} \cdot T_s}{R_L} \tag{4}$$

$$I_{in} \leq \frac{D_{CCM} T_s V_{in}}{2L_{in}} \tag{5}$$

$$D_2 = 1 - D_{DCM} \tag{6}$$

$$D_2 = \frac{K \cdot M}{D_{DCM}} \tag{7}$$

The converter operating conditions in BCM are more difficult to calculate. The converter switching frequency varies across the line cycle. According to [4] the converter switching frequency can be calculated as shown in (8). This approximation is made based on the assumption the inductor waveform is a triangular waveform with peak values ranging from zero amps to twice the converter input average current. Based on this assumption and knowing the instantaneous converter conditions and the inductance value, it is possible to calculate the converter switching frequency across the line cycle.

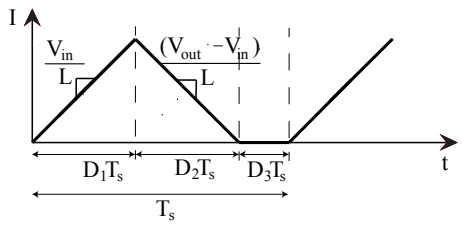

Fig. 3. Boost DCM inductor current waveform

$$f_{sw} = \frac{\left(V_{pk}/\sqrt{2}\right)^2 \left(V_{out} V_{pk} \sin \omega t\right)}{2LP_{out} V_{out}} \tag{8}$$

However, this prediction of the switching frequency has some limitations. Most of the converters operating in BCM or transition mode, make use of the valley switching operation [5], [6], [7]. This operation mode detects in different ways the inductor zero crossing current condition after the diode becomes reversed biased. When the current reaches zero, the MOSFET output capacitance resonates with the input inductor, making it possible to recover part of the energy stored on the device parasitic capacitance. The inductor current can be defined again using the current waveform presented in Fig. 4, where the period t_{valley} represents the valley switching period. The presence of this resonant period produces a mismatch on the calculated switching frequency. This mismatch becomes more evident as the resonant part of the inductor current increases with respect to the amount of power being transferred to the output. Fig. 5 shows a PFC converter operating in BCM mode. The converter is implemented using a $650\,V$ superjunction switch with a silicon carbide (SiC) diode. The converter switching frequency is $f_{sw} = 480\,kHz$. It can be observed that the valley switching subinterval uses a considerable part of the converter switching period. Moreover, in this case, the characteristic capacitance present in the vertical structure in superjunction devices produces a large time delay, since the MOSFET gate is turned off until the drain to source voltage rises to the final value. Therefore, using (8) will produce inaccurate estimation of the converter switching frequency under these conditions.

In this work, both the valley resonant period and the switch drain voltage rise time are considered in order to obtain a more accurate prediction of the converter switching frequency. The current and voltage during these periods are calculated using (9) and (10), respectively where I_c and V_c are the capacitor current and voltage. The non-linear capacitance voltage dependence is considered by interpolating from the manufacturer datasheet values, although curve fitting is also possible as previously presented in the literature [8], [9].

$$I_c(t) = I_c(0)\cos(\omega_0 t) + \frac{V_c(0) - V_{in}}{L\omega_0}\sin(\omega_0 t) \tag{9}$$

$$V_c(t) = (V_c(0) - V_{in})\cos(\omega_0 t) + \frac{I_c(0)}{C\omega_0}\sin(\omega_0 t) \tag{10}$$

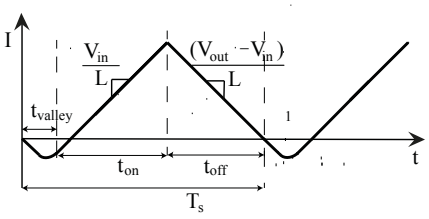

Fig. 4. Boost BCM inductor current waveform

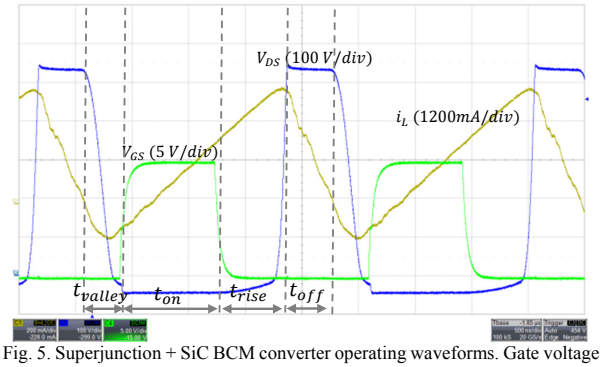

Fig. 5. Superjunction + SiC BCM converter operating waveforms. Gate voltage waveform (green 5V/div), drain voltage waveform (blue 100V/div) and inductor current waveform (yellow 200mA/div). Time scale: 500ns/div.

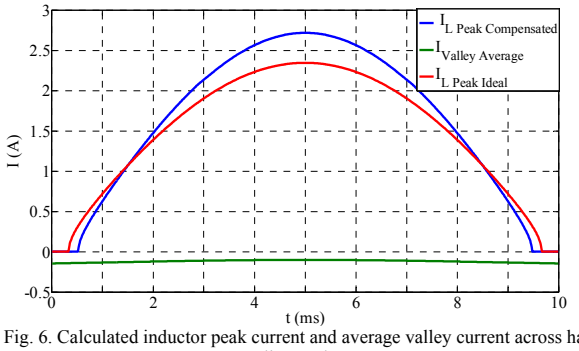

Fig. 6. Calculated inductor peak current and average valley current across half line cycle

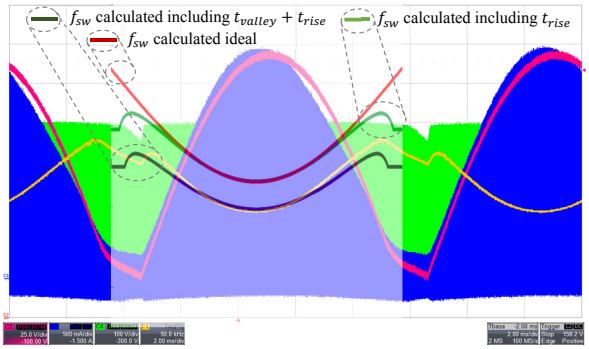

Fig. 7. Measured operating waveforms for a PFC boost converter. Drain to source voltage waveform (green 100 V/div), input voltage waveform (red 25 V/div, inductor current waveform (blue 500 mA/div) and switching frequency (yellow 50 kHz/div). Time scale: 2ms/div.

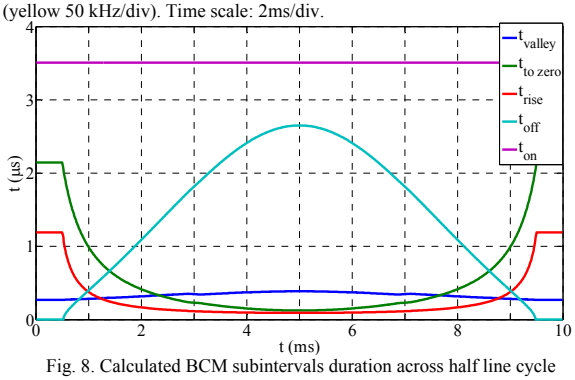

Fig. 8. Calculated BCM subintervals duration across half line cycle

Fig. 6 shows the calculated inductor peak current across half line cycle for the ideal case (red trace) where the peak value is equal to twice the required average input current. The green trace shows the average valley switching negative current. This portion of negative current increases the required switch on time in order to transfer the required amount of power to the converter load. Blue trace shows the effect of the negative valley current on the peak inductor current. Fig. 7 shows the measured converter waveforms and switching frequency for the conditions shown in Table I. The PFC controller operates with valley switching detection based on differentiation of the inductor voltage at the switch turn off. Superimposed with the measurement, the calculated switching frequency can be compared to the measured converter switching frequency. The red calculated trace corresponds to the ideal switching frequency calculated using (8). The green trace shows the effect of the MOSFET output capacitance charge at turn off. This effect becomes evident towards the input voltage zero crossings. Under these conditions, the fixed switch on time of the voltage control loop builds a small amount of current in the input inductor (due to the low instantaneous V_{in} value) creating a delay at the MOSFET turn off. The dark green trace includes the effect of the negative current flow created by the valley switching operation. As it can be observed, the switching frequency deviation becomes very significant across the whole line cycle. This calculation also includes the input decoupling capacitor effect on the converter switching frequency. As the operation approaches the zero voltage crossings of the rectified input voltage waveform, the positive current build up in the inductor is not enough to charge the MOSFET output capacitance up to the converter output voltage value, and the converter stops transferring power to the output. In this model it is considered that the converter input voltage remains constant at this value until the grid voltage is higher than the input capacitor voltage in the next cycle. However, as can be seen in Fig. 7, close to the input voltage zero crossings, the MOSFET drain voltage (green trace) and the input capacitor voltage (red trace) decrease due to the effect of the converter power losses. Fig. 8 presents the calculated subinterval times across the line cycle for the operating conditions shown in Fig. 7. As it can be seen, the MOSFET on time is considered to be constant across the cycle, but the off time decreases towards the input voltage zero crossings, which in the ideal case would create a switching frequency variation from the minimum switching frequency (11) to the maximum (12). However, as the operation approaches the zero crossings, the time the MOSFET drain to source voltage takes to rise (t_{rise}) and the time the inductor current takes to return to zero after the valley

TABLE I
SYSTEM SPECIFICATIONS AND COMPONENTS

Input voltage	$V_{in} = 120\ V_{rms}$
Output voltage	$V_{out} = 387\ V$
Output power	$P_{out} = 100\ W$
Input inductor	$P_{out} = 100\ W$
MOSFET	IPL65R130C7 650V superjunction Infineon
Diode	IDL10G65C5 SiC Infineon
Controller	FAN9612 BCM

$$f_{sw,min} = \frac{1}{(t_{on} + t_{off})} \quad (11)$$

$$f_{sw,max} = \frac{1}{t_{on}} \quad (12)$$

switching ($t_{to\,zero}$) increase, reducing the ideal converter switching frequency. The valley time subinterval remains almost constant during the whole cycle. The small deviation is caused by the differentiator action over the MOSFET drain to source dv/dt at the turn off. When the drain to source voltage starts decreasing, the differentiator will rise and decrease down to zero when the voltage derivative slows down close to the V_{DS} minimum to ensure valley switching or ZVS operation. In this case, the model is adjusted to start the MOSFET on time when the derivative slows down to 50 mV/ns.

III. Experimental Results

In order to perform the devices characterization, a low inductive DPT is used. The prototype is implemented using a four layer PCB taking special care to minimize the main ac current loop and driver current loop stray inductances while taking care not to unnecessarily increase the switching node stray capacitance. Moreover, a low capacitive inductor [10], [11], [12] and a minimum intrusive current measurement method [13], [14], [15] is employed in order to minimize the inserted inductance in the main switching loop. Fig. 9 shows the implemented DPT designed to accommodate 8x8 mm PQFN packages. In order to obtain more accurate switching energy measurements, the switching node (18 pF) and the oscilloscope probe capacitances (13.9 pF) are measured to be removed from the energy loss measurements. Fig. 10 and Fig. 11 present the measured switching energy loss for two superjunction devices in combination with a SiC diode. The characterization is performed at a rail voltage $V_{DC} = 400\ V$.The amount of energy corresponding to the switching node and the oscilloscope probe (2.55 μJ @ $400V$) has been removed from the turn on loss measurement. In this way, it is possible to observe that the turn on loss measurement at zero current level is between 3.6 μJ and 3.7 μJ. This value corresponds to the energy dissipated during the resistive charge of the diode parasitic junction capacitance. Therefore, the same amount of energy stored on this capacitance will be dissipated on the MOSFET channel during the MOSFET turn on. The measured value is in agreement with the manufacturer datasheet, which claims 3.5 μJ stored energy on the device output capacitance at $V_R = 400\ V$. Observing Fig. 11, it can be seen that at zero current conditions during the MOSFET turn off, the amount of measured energy corresponds to the energy stored on the MOSFET output capacitance which will be dissipated at turn on. The zero current values in this measurement have been extrapolated from the rest of the current points in the measurement, since it is impossible to measure a turn off event with zero current level. Both the superjunction measurements are in good agreement with the manufacturer datasheet specified energy. The 130 $m\Omega$ device presents a turn off loss at zero current level $E_{oss} = 4\ \mu J$ compared to $E_{oss} = 4.2\ \mu J$ specified in the component datasheet, while the 230 $m\Omega$ device presents $E_{oss} = 2.5\ \mu J$ compared to $E_{oss} = 2.62\ \mu J$.

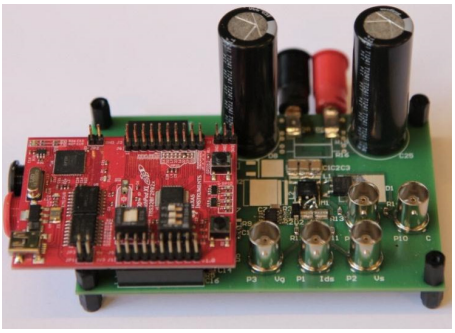

Fig. 9. Double pulse tester prototype

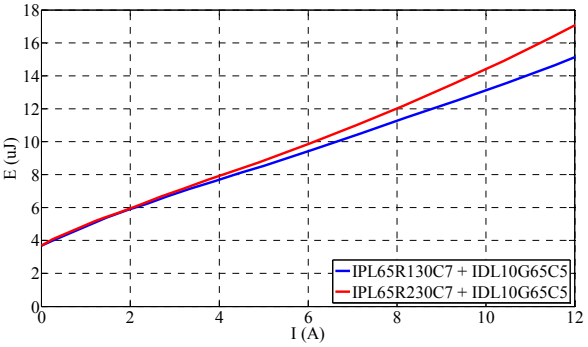

Fig. 10. Measured turn on energy loss

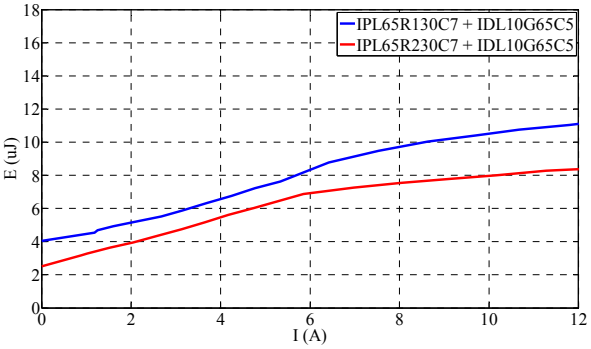

Fig. 11. Measured turn off energy loss

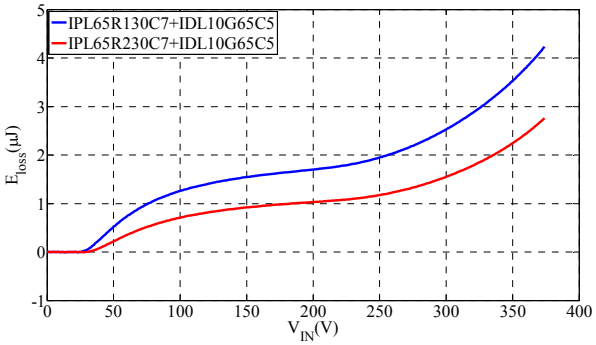

Fig. 12. Ideal capacitive loss at the switch turn on as a function of the converter input voltage

Fig. 12 shows the ideal amount of energy loss during valley switching operation of the converter. It can be seen that as the converter input voltage increases, the amount of recovered energy diminishes. On top of this energy loss, it has to be considered that the amount of energy delivered to charge the diode junction capacitance will be lost as resistive losses in the MOSFET channel. It is important to observe how the abrupt change in the superjunction MOSFET capacitance increases the turn on loss drastically even at low input voltage levels where the converter switching frequency will be higher. Moreover, most of the BCM controllers no matter if they are based on fixed delay time or differentiator will turn on the MOSFET when the capacitance abruptly changes and all the energy stored after this point will be lost. This will happen due to the fact that the capacitance change in the latest superjunction technology increases the value more than one order of magnitude. This fact produces the V_{ds} derivative to drastically slow down triggering the MOSFET turn on. In the same way, if a fixed delay time is used instead of a differentiator to decide the MOSFET turn on point in time, this delay time will be adjusted to catch the valley at higher V_{ds} voltages causing premature triggering at low input voltage levels.

IV. Evaluation

By using the DPT characterization data, and the presented models for a PFC, is possible to compare the performance of the different evaluated devices. The amount of energy recovered prior to the MOSFET turn on in BCM needs to be removed from the characterization energy curves. In order to do so, the code developed for estimating the converter switching frequency also calculates energy stored on the devices output capacitances. On top of that, the conduction losses in the semiconductors are calculated including the resonant currents during valley switching operation. In order to simplify the calculation, the MOSFETs characteristic on resistance and diode threshold voltage and dynamic resistance specified @25℃ in the manufacturer datasheets are used. Fig. 13 and Fig.14 show a CCM and BCM semiconductor loss calculation breakdown for IPL65R230C7 in combination with a SiC diode IDL10G65C5. The converter operates with $V_{in} = 230\ V_{rms}$ and $P_{out} = 200\ W$ for an output voltage level $V_{out} = 390\ V$. Both BCM and CCM calculations are plotted versus the selected input inductor value. As it can be observed in CCM, the diode

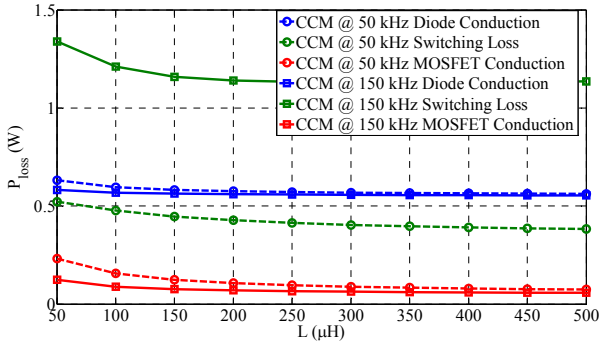

Fig. 13. Semiconductor power loss breakdown during CCM operation vs. input inductor value

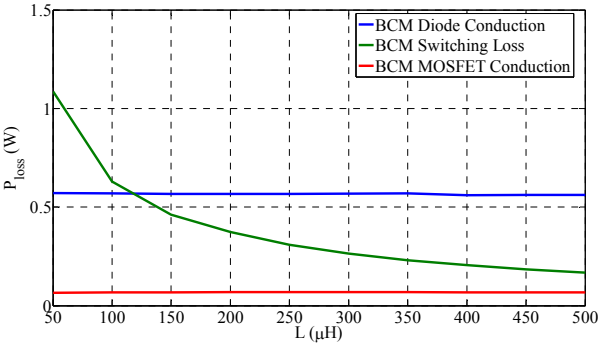

Fig. 14. Semiconductor power loss breakdown during BCM operation vs. input inductor value

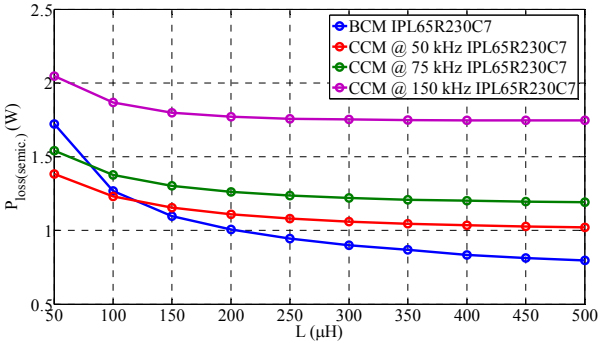

Fig. 15. Semiconductor power loss for IPL65R230C7 + IDL10G65C5 vs. input inductor value

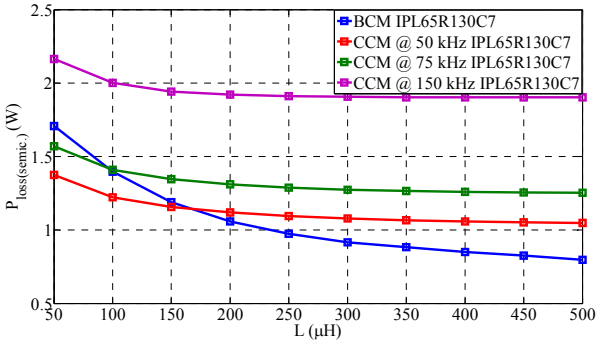

Fig. 16. Semiconductor power loss for IPL65R130C7 + IDL10G65C5 vs. input inductor value

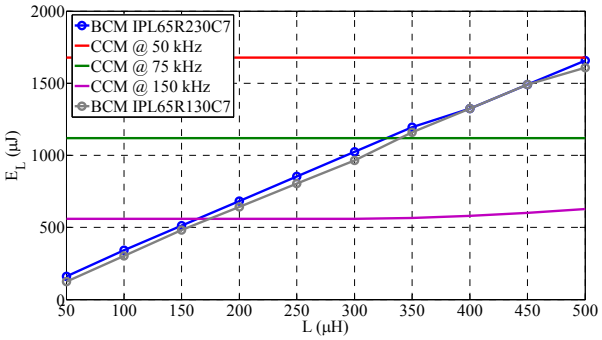

Fig. 17. Input inductor energy storage requirement vs. input inductance value for BCM and CCM operation

conduction loss is the predominant loss at low frequency levels. Increasing the input inductor value does not have a visible effect on this loss due to the fact that the main contribution to the loss in this component comes from the average current. It is only at very low inductance value where the rms component of the current has an effect on this loss. The MOSFET conduction loss at this power level and input voltage level contributes very little to the total final semiconductor loss. As the switching frequency and the inductance value increase, the MOSFET conduction loss diminishes due to the decreased rms component. The switching losses in CCM represent a large part of the total loss even at $f_{sw} = 50\ kHz$. Increasing the inductance value has a small effect on this loss due to the fact that the largest part of the loss at this voltage and power levels are capacitive losses. From Fig. 14, it seems clear that employing BCM operation mode will slightly increase the semiconductor conduction losses while reducing capacitive switching losses.

Fig. 15 and Fig.16 present a comparison of IPL65R230C7 and IPL65R130C7 in combination with the SiC diode IDL10G65C5 in CCM and BCM operating modes, while Fig. 17 present the input inductor energy storage requirement (13) which gives an estimation for comparison purposes of the input inductor size.

$$E_L = \frac{{I_{L,peak}}^2 L}{2} \tag{13}$$

From this comparison, it can be seen that when the input inductor value is around $L \approx 150\ \mu H$ the BCM operation presents equal or lower semiconductor losses than the CCM solutions $@\ f_{sw} = 50\ kHz$ due to the capacitive switching loss reduction. Moreover, the input inductor size is reduced more than three times.

V. Conclusion

This paper presents an evaluation procedure to compare different PFC solutions operating in both CCM and BCM. The evaluation is based on DPT measurements combined with a detailed model for prediction of the converter switching frequency across the input line cycle. By combining these tools it is possible to predict the semiconductor performance and the attainable advantages that can be obtained in terms of power density/efficiency by inserting a new semiconductor technology.

This works presents a case study where two state-of-the-art Si MOSFETs C7 are evaluated with a G5 SiC diode in both modes. The obtained results show that the valley switching combined with the ZCS turn on present in this operation mode, overcomes the current stress increment and makes it possible to increase the converter switching frequencies attaining a large reduction on the converter magnetic storage requirement.

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F

A Comparison between Boundary and Continuous Conduction Modes in Single Phase PFC Using 600V Superjunction Devices

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A Comparison between Boundary and Continuous Conduction Modes in Single Phase PFC Using 600V Range Devices

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***Abstract*— This paper presents an analysis and comparison of boundary conduction mode (BCM) and continuous conduction mode (CCM) in single phase power factor correction (PFC) applications. The comparison is based on double pulse tester (DPT) characterization results of state-of-the-art superjunction devices in the 600V range. The measured switching energy is used to evaluate the devices performance in a conventional PFC. This data is used together with a mathematical model for prediction of the conducted electromagnetic interference (EMI). This allows comparing the different devices in BCM and CCM operation modes and evaluating the performance as a function of the PFC power density and efficiency.**

***Keywords*— Power factor correction (PFC), boundary (BCM), continuous conduction mode (CCM), conducted EMI, power density, efficiency, evaluation**

I. INTRODUCTION

Power factor correction (PFC) circuits are widely used in industrial and household applications to fulfill the power factor and harmonic standards. This type of circuits are traditionally used in continuous conduction mode (CCM) configuration, however, nowadays the boundary conduction mode (BCM) solution has become a highly adopted solution because of its control scheme simplicity. The main disadvantage of converters operating in BCM is the increased inductor ripple that increases the differential mode input EMI filter requirement. Moreover, the current stress in all the components is increased, which negatively affects the converter conduction losses. On the other hand, the inductor size is reduced compared to CCM operation and the switch turn-on losses can be heavily reduced with zero current switching (ZCS) and valley switching to recover part of the energy stored in the switch output capacitance.

BCM operation has gained interest since the introduction of cascode 650 V Gallium Nitride (GaN) devices. These devices are formed by using a cascode connected low voltage silicon (Si) MOSFET with a normally on GaN switch. The interconnection of these devices makes cascode structures to present very low turn-off loss, which is almost independent of the current level [1]. This phenomenon happens because the output capacitance of the low voltage side MOSFET and the input capacitance of the GaN switch get charged in parallel by the load current at the turn-off event, minimizing the GaN channel turn-off losses. Therefore, switches configured in cascode structure are very attractive for high frequency BCM operation, since the increased current level at the main switch turn-off event will have very little effect on the converter switching losses [2]. Moreover, GaN devices in cascode structure are very attractive for synchronous rectification applications due to the reduced reverse recovery compared to 600 V Si super junction structures. The reverse recovery energy corresponds to that of the low voltage MOSFET in the cascode configuration, and according to [2], this energy is a couple of orders of magnitude smaller than that of a vertical super junction Si device. The possibility of using synchronous rectification allows to further extend the operating power range of BCM converters, which makes this operation mode even more attractive.

In order to analyze the attainable advantages by using different semiconductor devices in PFC applications operating in CCM and BCM, it is necessary to evaluate the semiconductor loss and to compare the solutions in terms of converter power density. The semiconductor conduction loss can be calculated from the data provided in the manufacturer datasheets, but the switching loss needs to be evaluated and characterized. On the other hand, a mathematical model for prediction of the conducted EMI noise needs to be used to evaluate and compare the input filter requirement for different case studies. This paper presents a design oriented methodology for power factor corrector implementation based on double pulse tester (DPT) dynamic characterization to evaluate the switch-diode pair energy loss. Using this data and the manufacturer datasheets, the semiconductor switching and conduction loss can be calculated for half a line cycle. At the same time, the inductor size can be estimated based on the energy requirement ($1/2 \cdot I_{peak}^2 \cdot L$). The input filter requirement can be evaluated based on the calculated quasi peak and peak noise from the calculated harmonics across half the line cycle.

II. DYNAMIC CHARACTERIZATION

The devices dynamic characterization is performed in a low inductive DPT. This circuit is the basic configuration used to evaluate the dynamic performance of different switches

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technologies under clamped inductive load operation. The prototype has been designed to minimize the parasitic inductances and capacitances in the switching loop [3]. The main switch current is measured using a flat current shunt structure to minimize the parasitic inductance inserted in the loop and maximize the current measurement bandwidth.

The characterization procedure is the same followed in [4]. The CCM switching losses can be directly extracted from the double pulse tester measurements (Fig. 1). The BCM turn-off losses are obtained directly from the DPT measurements as well, but the turn-on losses are reduced compared to the measurements due to the valley switching operation. In order to obtain the MOSFET switching loss for BCM operation, the energy loss is measured under zero current switching conditions at the turn-on and turn-off events. Under zero current conditions the energy loss measurement at turn-on will correspond to the diode junction capacitance energy. In the same way, under zero current conditions at turn-off, the energy corresponds to the MOSFET output capacitance stored energy. Once these values are obtained, it is possible to estimate the MOSFET-diode pair performance under valley switching operation if the amount of energy loss at turn-on and energy recovered during the valley switching subinterval are calculated as a function of the converter input voltage (Fig.2).

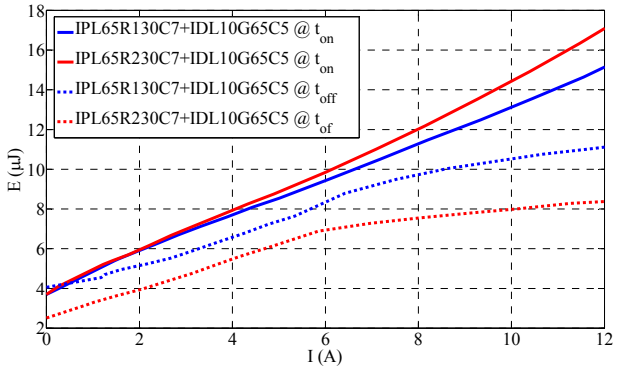

Fig. 1. Measured turn-on and turn-off energy loss as a function of the current level

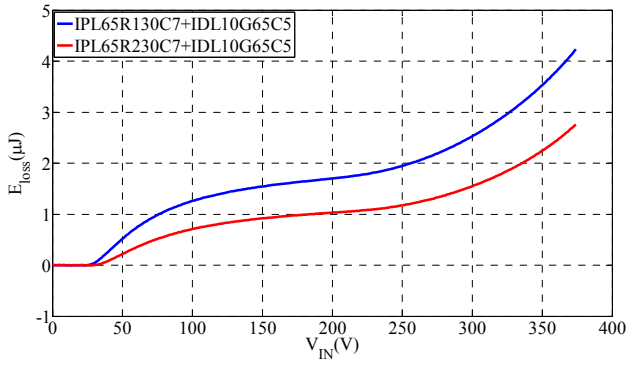

Fig. 2. Calculated remaining turn-on energy loss under BCM operation as a function of the converter input voltage

III. CONDUCTED EMI PREDICTION

Using a mathematical model for conducted EMI prediction enables to directly compare the EMI filter requirements for both CCM and BCM operation modes. This paper uses a mathematical model based on the work presented in [5], [6] to calculate the quasi peak conducted EMI noise under boundary and continuous conduction mode operation for a conventional single phase PFC, as shown in Fig 3. In CCM mode, the input current waveform can be defined according to the converter input voltage and the output power requirement. For the CCM operation mode deriving the inductor current is a straight forward calculation [7], but for the BCM mode, the switching frequency varies across the line cycle. This switching frequency can be calculated according to [6] as shown in (1).

$$f_{sw} = \frac{\left(V_{pk}/\sqrt{2}\right)^2 \left(V_{out} V_{pk} \sin \omega t\right)}{2LP_{out}V_{out}} \qquad (1)$$

However, the switching frequency is affected by the MOSFET and diode output capacitances, as shown in Fig. 4. As it can be observed, at low inductor current levels the charge of the MOSFET output capacitance creates a delay from the gate turn-off event until the inductor starts to discharge. Moreover, at the end of the inductor discharge, when the current level reaches zero and the output diode becomes reverse biased, the valley switching interval will create an extra delay and a negative current flow in the input inductor that affects the ideally calculated converter switching frequency [4], [8].

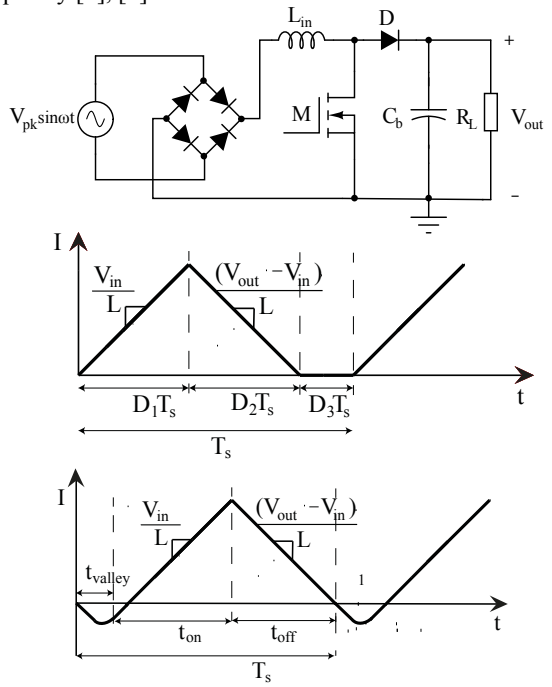

Fig. 3. Conventional PFC schematic and inductor current waveform used for definition of the CCM/DCM and BCM operating modes

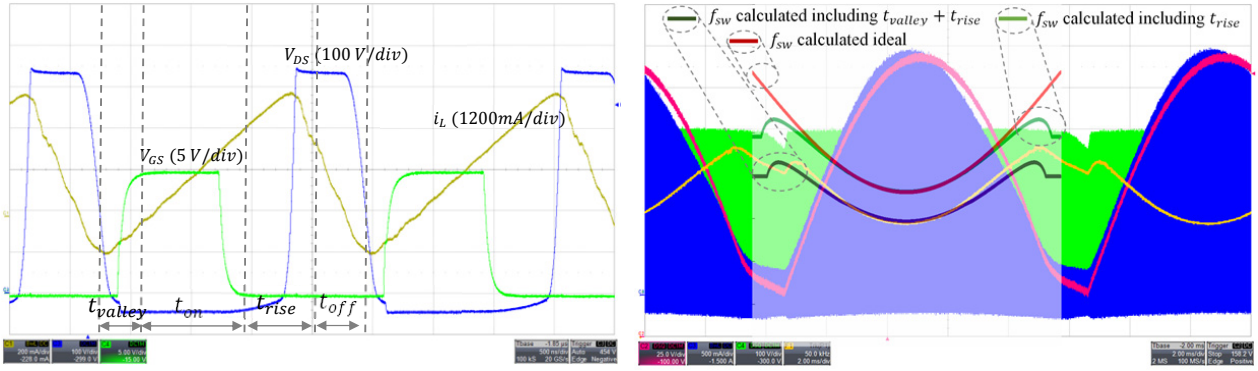

Fig. 4. Left, PFC BCM operating waveforms 500ns/div. Gate waveform (green 5V/div), drain waveform (blue 100V/div) and inductor current (yellow 200 mA/div). Right, MOSFET drain waveform (green 100 V/div), input voltage after the rectifier (red 25V/div), inductor current (blue 500 mA/div) and converter switching frequency variation across line cycle. Yellow measured, red ideally calculated and black taking switching node capacitance into consideration.

The switching frequency across the line cycle can be calculated taking into account the resonant periods between the input inductor and the switching node capacitance. In order to do so, the semiconductor parasitic capacitance can be extracted from the manufacturer datasheet, or measured using the setup shown in Fig. 5. Using a dc blocking capacitor it is possible to measure the variation of the capacitances as a function of an applied dc voltage. Fig. 6 shows the measured capacitance for a MOSFET-diode pair and the PCB switching node parasitic capacitance. The inductor current shape and converter switching frequency are calculated for half line cycle and the harmonics of the inductor current are calculated by approximating the inductor current shape to a pure triangular waveform to simplify the Fourier analysis. Fig. 7 shows a comparison of an average and quasi peak measurement performed over the inductor current of a single phase conventional PFC converter with the conditions shown in Table I.

TABLE I
SYSTEM SPECIFICATIONS AND COMPONENTS

Input voltage	$V_{in} = 120\ V_{rms}$
Output voltage	$V_{out} = 389\ V$
Output power	$P_{out} = 100\ W$
Input inductor	$L = 220\ \mu H$
MOSFET	IPL65R230C7 650 V
Diode	IDL10G65C5

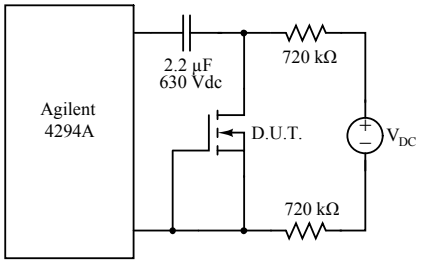

Fig. 5 Semiconductor parasitic capacitance measurement setup

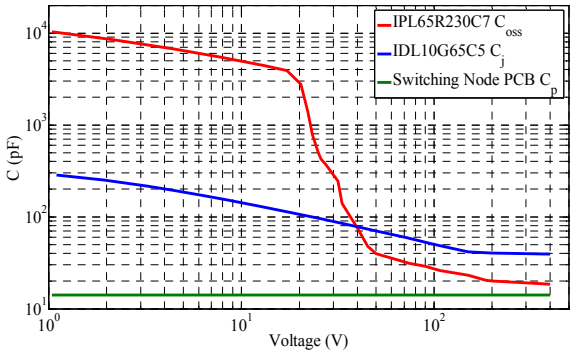

Fig. 6. Measured capacitance of the components connected to the converter switching node

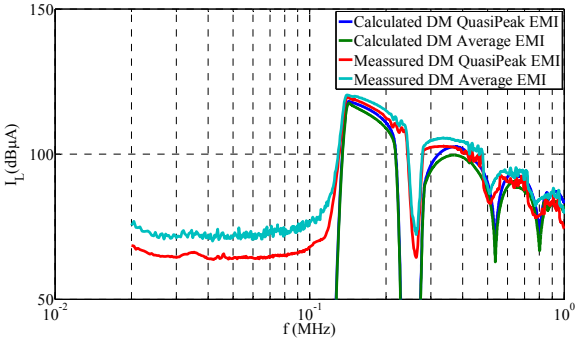

Fig. 7. Measured and calculated inductor current conducted EMI

Once the model for calculating the inductor current harmonics has been verified, the harmonics at the measurement point can be calculated by using the equivalent LISN network transfer function. With the calculated LISN network measurement point voltage is possible to calculate the necessary attenuation requirement for fulfilling the conducted standards. At the same time, thanks to the semiconductor characterization data, and the definition of the input inductor current shape across the line cycle, the semiconductor and switching loss can be estimated together with the input inductor energy storage requirement. In this way is possible to perform a comparison of the evaluated devices in BCM and CCM operating modes.

IV. EVALUATION

In this section, a case study for a single phase PFC using the superjunction IPL65R230C7 device with the IDL10G65C5 SiC diode is analyzed. The converter input voltage is $V_{in,rms} = 230\,V$ and the input power is $P_{in} = 200\,W$. The semiconductor pair is evaluated for both CCM and BCM operating modes for an input inductor value ranging from $L_{in} = 100 - 500\,\mu H$ and for a two stage pi filter at the input of the converter as shown in Fig. 8

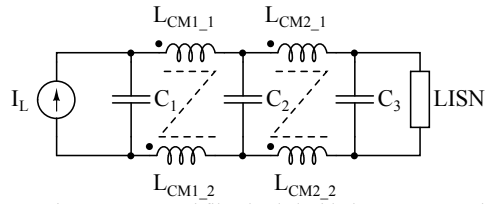

Fig. 8 Two stage pi filter loaded with the LISN network

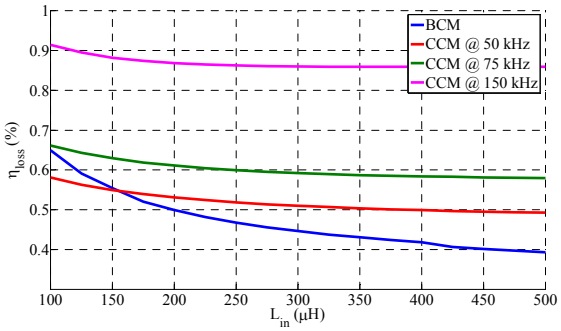

Fig. 9 Semiconductor efficiency loss vs. input inductance value

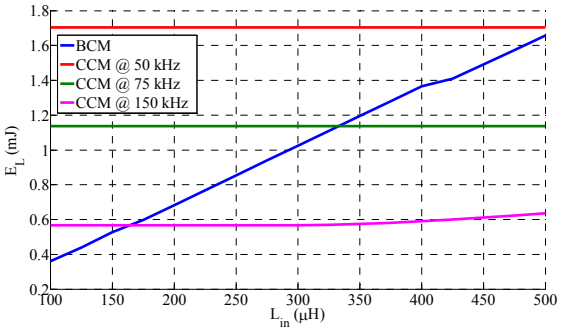

Fig. 10 Input inductor energy strorage requirement vs. input inductance value

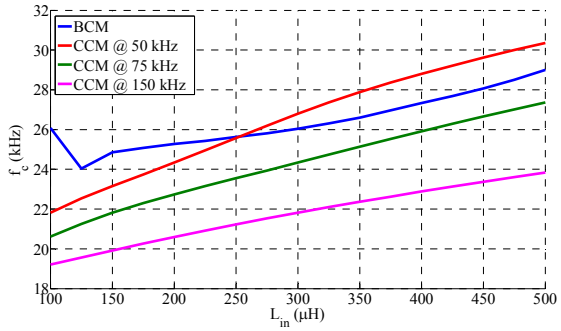

Fig. 11 Input filter corner frequency vs. input inductance value

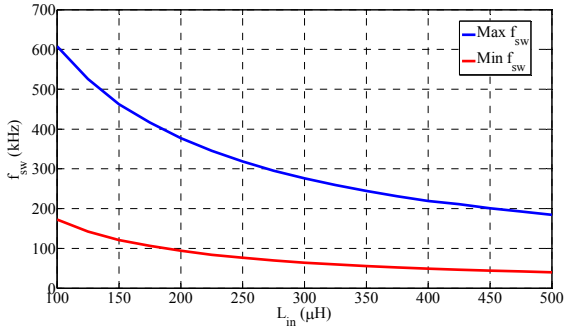

Fig. 12 BCM converter switching frequency vs. input inductance value

Fig. 9 shows the calculated semiconductor efficiency loss as a function of the selected input inductor values for BCM and three different CCM switching frequencies. In the BCM case, as the input inductor value is reduced, the converter switching frequency increases having a negative impact on the semiconductor switching losses. For the CCM cases, as the input inductor value is reduced for the same switching frequencies, the semiconductor loss is increased due to the increased current stress through the semiconductors. It is interesting to see that for this power level, when the input inductor is over 150 µH, the BCM presents the lowest semiconductor loss of all four solutions.

Fig. 10 shows the input inductor energy storage requirement. It can be observed, that for the BCM case at 150 µH, the energy storage requirement is very similar to the CCM at 150 kHz but with almost half the semiconductor loss, and almost three times smaller than the energy storage requirement compared to the CCM case at 50 kHz with similar semiconductor losses.

Fig. 11 presents the calculated corner frequency for the two stage pi filter selected for this analysis. It is interesting to see how only the CCM solution at 50 kHz is able to increase the input filter corner frequency respect to the BCM solution. Increasing the CCM operation frequency does not relax the input filter corner frequency requirement because the third and the second harmonic of the converter switching frequency get into the measurement range. In the BCM case, there exists an absolute minimum corner frequency when the input inductor value is equal to 125 µH. As can be seen in Fig. 12, when the input inductor is at this value, the minimum converter switching frequency reaches 150 kHz which corresponds to the initial frequency in the conducted EMI measurement range. It is important to observe that in BCM mode, the minimum operating frequency corresponds with the peak of the sinusoidal voltage waveform when the inductor current harmonics possess the highest value. As a conclusion, it can be said that the BCM operation is a good candidate for reducing input inductor size while maintaining a low semiconductor loss when compared to the conventional CCM operated converter under 50 kHz switching frequency. If both the input inductor and the input filter size need to be reduced respect to the conventional CCM implementation, MHz range BCM implementations need to be the adopted in order to push the converter minimum switching frequency at maximum power level far away from the beginning of the measurement range.

V. CONCLUSION

This paper presents a comparison of CCM and BCM modes in single phase PFC applications by evaluating the two operating modes in terms of power density and efficiency. The proposed method uses DPT dynamic characterization results together with the characterized devices' characteristic output capacitance in order to calculate the PFC switching losses through half line cycle both in CCM and BCM conduction modes. This makes it possible to analyze the converter performance for different inductance values and switching frequencies, which in combination with the analytical CCM and BCM conducted EMI models, enables a converter efficiency and power density comparison for different state of the art 600V range devices.

As previously shown in [5] and [4], BCM with valley switching operation, makes prediction of the converter switching frequency a complicated task. In order to obtain accurate results, the resonance periods at the valley interval and at the switch turn off event need to be taken into account. This can be done by obtaining the parasitic capacitances connected to the converter switching node.

The case study analyzed in this work shows that BCM operation mode helps reducing the converter semiconductor loss compared to the CCM implementations. This is due to the fact that, although the current stress through the semiconductors is increased respect to CCM implementations (producing an increased semiconductor conduction loss), the turn-on under ZCS and valley conditions, produce a bigger reduction on the semiconductor switching loss. Moreover, BCM makes it possible to achieve a great reduction in the input inductor energy storage requirement, when compared to conventional 50 and 75 kHz CCM implementations. However, concerning the input filter corner frequency requirement, a reduction in the size compared to a 50 kHz CCM implementation is only possible when the BCM implementation operates in MHz switching frequency range.

Observing Fig. 9 and 12, it can be seen that using these devices in MHz switching frequency range will produce a large penalty in the semiconductor efficiency loss. As it can be observed in Fig. 2, the non-linear capacitance characteristics in superjunction devices, makes this technology not the best option for high frequency BCM implementations. This non-linear capacitance with an abrupt increment at low voltage levels, produces an increment of the semiconductor capacitive switching losses under valley switching operation. On the other hand, GaN implementations in this voltage range help reducing capacitive switching losses under valley operation. Moreover, the cascode configuration with its intrinsic turn-off mechanism makes this technology a firm candidate in BCM MHz implementations pursuing high power density and efficiency.

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Zero Voltage Switching Control Method for MHz Gallium-Nitride based Boundary Conduction Mode Converters

Ready to be submitted to Transactions in Power Electronics (TPEL)

Zero Voltage Switching Control Method for MHz Gallium-Nitride based Boundary Conduction Mode Converters

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ABSTRACT

Boundary conduction mode (BCM) or critical conduction mode (CrM) converter implementations have become very attractive since the introduction of gallium nitride (GaN) switches. This operation mode is characterized by an inductor current that operates in the boundary between continuous (CCM) and discontinuous conduction modes (DCM) making the converter switching frequency dependent on the converter operating conditions. The advantage of this operation mode versus CCM is achieving zero current switching (ZCS) conditions for the converter rectifier, which makes it possible to use silicon (Si) based rectifiers without having a penalty due to reverse recovery issues. Moreover, the main switch turn-on loss is decreased due to ZCS conditions and valley switching operation. However, the penalty is an increased current stress in the circuit, and an increased main switch turn-off energy loss. Implementation of synchronous rectifier in BCM converters makes it possible to achieve zero voltage switching (ZVS) conditions by extending the synchronous rectifier conduction time after zero current condition in the inductor. High power density, high efficiency MHz implementations have already been demonstrated in the literature; however, none of the proposed solutions solves the controllability issues of the synchronous rectifier switch. This work proposes and validates a ZVS adaptive control method for BCM converters operating in the MHz switching frequency range.

***Index Terms*—Adaptive control, zero voltage switching (ZVS), boundary conduction mode (BCM), high switching frequency, high efficiency.**

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I. INTRODUCTION

Switched-mode power supplies (SMPS) technology has been an efficient solution for voltage and current conversion applications from the early 20th century. Compared to linear regulators, SMPS can ideally reach efficiencies up to $\eta = 100\,\%$. This technology, based on the combination of reactive elements with any type of switch, was initially developed employing mechanical switches, vacuum tubes, and finally semiconductor based switches such as thyristors, bipolar junction transistors (BJT), and Metal Oxide Semiconductor Field Effect Transistors (MOSFET) [1], [2], [3]. The size and the cost of SMPS is heavily influenced by the size of the reactive energy storage elements, which is inversely proportional to the converter operating frequency. Therefore, increasing the converter switching frequency allows for an increased converter power density and reduced cost. However, the switches, far from being ideal, present switching losses that put a practical limit on the maximum attainable converter switching frequency. Resonant SMPS topologies present an alternative solution for eliminating the converter switching losses and increasing the power density [4], at the penalty of an increased current stress due to the increased reactive energy circulation in the circuits. However, the main driver for reduction of the size of the converters has always been semiconductor technology [5].

Silicon (Si) has been and still remains the main semiconductor for power electronics applications. However, Si semiconductor manufacturing has mature and optimized fabrication processes, and consequently, it is close to reaching the theoretical limits of the material [6]. Wide band-gap semiconductors present an increased electrical field strength compared to Si, making it possible to achieve lower specific on resistances for the semiconductor material compared to Si [7], [8], [9]. The reduction on the material specific on resistance makes it possible to shrink the semiconductor die sizes, which reduces the parasitic capacitances and enables faster switching speeds. The two main wide band-gap semiconductor materials being integrated into power semiconductor manufacturing processes are Gallium-Nitride (GaN) and Silicon Carbide (SiC). Both materials present a lower intrinsic carrier concentration than silicon, reducing leakage currents and making it possible to increase the operation temperature. Moreover, SiC material possess larger thermal conductivity than that of Si, and GaN presents a very stable R_{ds-on} over temperature [10] which makes both semiconductors ideal for high temperature,

high power density converter implementations. However, both GaN (100 €/cm^2) and SiC (10 €/cm^2) materials are expensive compared to Si material, which is down to 0.1 €/cm^2 [8].

Epitaxial grow of GaN on Si substrate brings GaN semiconductor manufacturing costs down because of the substrate price reduction and due to the fact that GaN on Si can use established Si manufacturing processes. Moreover, according to the attained size reduction compared to a Si switch, a GaN device could have a lower cost than the equivalent Si counterpart for the same ratings [9]. This price reduction makes GaN semiconductor a more economical solution for low and medium voltage applications than SiC. Several vendors have released GaN High Electron Mobility Transistors (HEMT) up to 650V operation range, although some manufacturers report 1.7 kV devices [10]. HEMT is a lateral device where a 2 dimensional electron gas (2DEG) forms in the junction between a GaN and an Aluminum GaN layer. Intrinsically, this is a normally on device, and several approaches have been adopted by manufacturers to produce a normally off device [10].

Comparing the available technologies in the 600/650V range, it can be seen that current GaN and SiC devices outperform in terms of R_{ds-on} per unit area the current state-of-the-art Si technology [11]. However, the maturity of existing Si technology, where modern vertical super junction structures have surpassed the predicted Si limit [12],[13], together with the room for optimization of manufacturing processes in wide band-gap semiconductors, makes the differences between materials to be far from the predicted figures from the material characteristics. Replacement of the current Si technology nowadays is heavily dependent on application and cannot be determined only by R_{DS-on} per unit area figure of merit. Nowadays, current GaN and SiC devices in the 600V range do not offer a considerable improvement in hard switched converter applications over Si vertical super junction structures in terms of switching losses caused by the energy stored in the device output parasitic capacitance [11],[14],[15]. However, in applications requiring synchronous rectification or in high frequency resonant converter applications, wide band-gap devices offer an improvement over Si. This is due to the effect of the body diode reverse recovery charge (Q_{rr}) and the output capacitance charge (Q_{oss}) in Si super junction switches. Moreover, as presented in [16] and [17], vertical super junction structures present an hysteresis loss during the charge and discharge of the device parasitic output capacitance that is inversely proportional to the R_{ds-on} per

unit area, which makes state-of-the-art super junction switches non suitable for high frequency resonant operation.

Cascode structures are widely used to produce normally off GaN devices in the 600V range. This cascode structure is constructed with a normally on GaN HEMT configured with a low voltage Si MOSFET as shown in Fig.1.

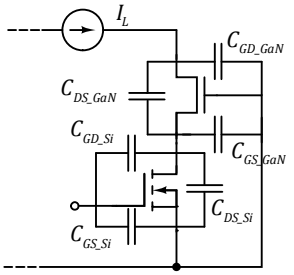

Fig. 1. GaN-Si cascode structure with parasitic capacitances

As presented in [18] and [19], when a proper balanced cascode structure is constructed, the switch will present a current load driven turn-off mechanism, where the load current charges the Si switch output capacitance in parallel with the GaN input capacitance. This produces the turn off energy loss to be almost independent of the load current level. This behaviour makes the GaN HEMT-Si cascode structure to be a perfect candidate for BCM implementations where valley or ZVS can be achieved. High frequency BCM GaN based implementations have been demonstrated in the literature, where the increased conduction loss due to the increased current stress in BCM implementations is compensated by the reduction in switching loss [20]. In [19] a 5 MHz ZVS boost BCM implementation with efficiency figures up to $\eta = 98\%$ is demonstrated. As presented in [21] and [22], MHz implementations allow for a large reduction of the converter input inductor and filter which heavily affects the converter power density. However, pushing the converter switching frequency in BCM implementations is only possible when the converter operates under ZVS conditions, which depend on the converter input to output voltage ratio and the non-linear switching node parasitic capacitance. In [23] a ZVS extension method for BCM converters with synchronous rectification is presented. In this solution, the synchronous rectifier time is increased to create a negative inductor current to discharge the switching node capacitance achieving ZVS independently of the converter input to output voltage ratio. A MHZ BCM boost derived power factor

correction circuit is demonstrated in [24] with ZVS extension. However, both of the proposed prototypes, relay on prototype measurements and characterization to map the necessary negative inductor current to achieve ZVS as a function of the converter input to output voltage. This is a time consuming procedure where components tolerance will create errors that will result in loss of ZVS conditions or increased components current stress. This paper presents an adaptive control method for ZVS extension where the switching node voltage is regulated in close loop control by controlling the synchronous rectifier conduction time. The proposed control method is demonstrated in a GaN MHz boost BCM implementation.

This paper is organized into five sections: After the introduction presented in Section I, Section II presents the BCM operation both under valley and extended zero voltage switching mode operation, and the equations that define the converter operation under these modes. Section III presents the proposed adaptive control method for ZVS extension operation, and Section IV shows the implemented prototype. Finally, the conclusion is presented in section V.

II. BOUNDARY CONDUCTION MODE OPERATION

Boundary conduction mode corresponds to an operation mode where the converter inductor current operates between the continuous and the discontinuous conduction modes. The ideal inductor voltage and current waveform are shown in Fig. 2. In this operation mode, the converter switching frequency varies as presented in [25] according to (1) where M is defined as the converter input to output voltage ratio as in (2) for a conventional boost converter.

$$f_{sw} = \frac{{V_{in}}^2(1-M)}{2LP_{out}} \tag{1}$$

$$M = V_{in}/V_{out} \tag{2}$$

However, during boundary conduction mode, valley switching or ZVS at the turn on of the main switch are preferred to reduce the semiconductor switching losses. As the converter switching frequency is increased, the valley switching or ZVS time and the switching node rise time need to be taking into account to accurately predict the converter switching frequency [26], [21], [22].

A. Valley Switching Operation

A conventional boost converter with the typical valley switching waveforms under boundary conduction mode operation is depicted in Fig. 2. When the inductor current decreases to zero at t_3, the rectifier becomes reverse biased, and the parasitic capacitances attached to the switching node resonate with the input inductor. The equivalent circuit during the resonant period, can be simplified to an ideal LC circuit where the MOSFET output parasitic capacitance (C_{oss}) appears in parallel with the diode junction capacitance (C_j) and resonate with the converter input inductance with angular frequency ω_o as denoted in (3).

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{3}$$

Where $C = C_{oss} + C_j$

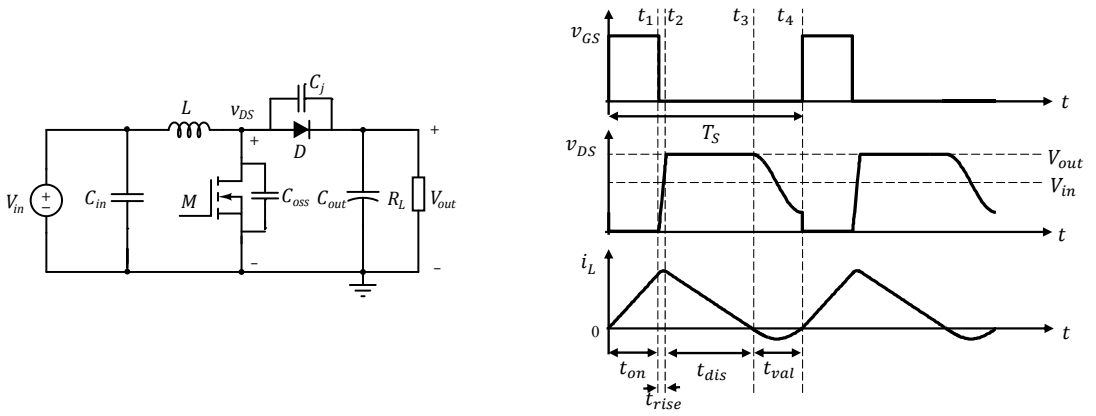

Fig. 2. Conventional Boost PFC with BCM valley switching operating waveforms.

The ideal equivalent circuit used to describe this resonant interval is presented in Fig. 3 *a*). As it can be observed in Fig. 3 *b*), in conventional BCM boost implementations, if the switching node capacitance is assumed to be ideal, the boost switch will lose its ability to soft switch when the converter input voltage V_{in} is higher than $V_{out}/2$ or $M > 0.5$.

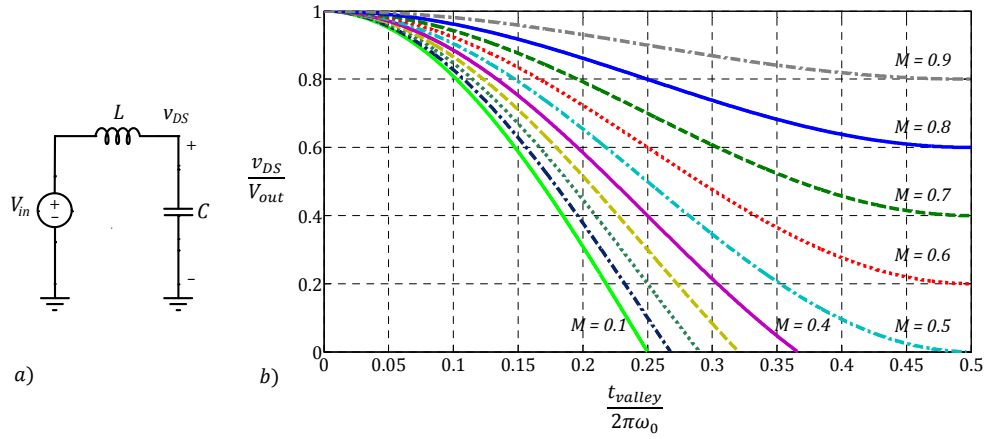

Fig. 3. Equivalent resonant circuit a) and b) switching node voltage vs. time for different voltage ratios M.

The set of equations that describe the voltage and the current in this equivalent LC circuit are presented in (4) and (5).

$$i_L(t) = \frac{V_{in} - v_{DS}(0)}{L \cdot \omega_0} sin(\omega_0 t) + i_L(0) \cdot cos(\omega_0 t) \tag{4}$$

$$v_{DS}(t) = (v_{DS}(0) - V_{in}) \cdot cos(\omega_0 t) + V_{in} + \frac{i_L(0)}{C \cdot \omega_0} sin(\omega_0 t) \tag{5}$$

At the beginning of the switching period, the inductor current is increased from zero value with $di_L/\mathrm{dt} = V_{in}/L$. Assuming an ideal switch action, after the switch is turned off at t_1, a resonant interval takes place where the switching node voltage will increase until the rectifier diode becomes forward biased. The voltage and current waveform in the t_{rise} interval can be described by using (4) and (5) and particularizing for $v_{DS}(0) = v_{DS}(t_1) = V_{out}$ and $i_L(0) = i_L(t_1)$ where:

$$i_L(0) = i_L(t_1) = \frac{V_{in}}{L} t_{on} \tag{6}$$

The duration of this interval t_{rise} can be calculated as shown in (7) by solving for the time at which the node voltage equation $v_{DS}(t)$ is equal to the converter output voltage V_{out}. This expression is valid as long as a minimum inductor current at the beginning of the interval (8) ensures the switching node voltage reaches the converter output voltage V_{out}.

$$t_{rise} = \frac{1}{\omega_0} arctan\left(\frac{1}{\omega_0} \frac{i_L(t_1) \cdot (1 - M) + V_{in}\sqrt{(2M-1)C/L + (i_L(t_1)/V_{out})^2}}{M(M-1)C/L + i_L(t_1)\sqrt{(2M-1)C/L + (i_L(t_1)/V_{out})^2}}\right) \tag{7}$$

$$i_L(t_1) \geq \sqrt{C/L}\,(V_{out} - V_{in}) \tag{8}$$

At t_2, the rectifier diode becomes forward biased and the inductor discharges down to zero with $di_L/\mathrm{dt} = (V_{out} - V_{in})/L$. The duration of this interval can be calculated as:

$$t_{dis} = \frac{i_L(t_2)}{(V_{out} - V_{in})/L} \tag{9}$$

When the inductor current reaches zero, the valley switching interval starts. During this interval, part of the energy stored in the parasitic capacitance of the switching node will be transferred back to the input inductor. The input inductor current waveform and the switching node voltage waveform during the valley switching interval can be described using (4) and (5) respectively, particularizing for the initial conditions $v_{DS}(0) = v_{DS}(t_1) = V_{out}$ and $i_L(0) = i_L(t_3) = 0$. The duration of this interval can be calculated as shown in (10).

$$t_{val} = \frac{\pi}{\omega_0} \tag{10}$$

B. Natural Zero Voltage Switching Operation

When the converter input voltage V_{in} is smaller than $V_{out}/2$ or $M < 0.5$, the boost switch will operate under ZVS conditions as shown in Fig. 4. During this operation mode, all the energy stored in the switching node parasitic capacitance is recovered before the boost switch turn on event. The time to reach ZVS conditions t_{zvs} can be calculated from (5) for $v_{DS}(0) = v_{DS}(t_4) = V_{out}$ and $i_L(0) = i_L(t_4) = 0$ as shown in (11).

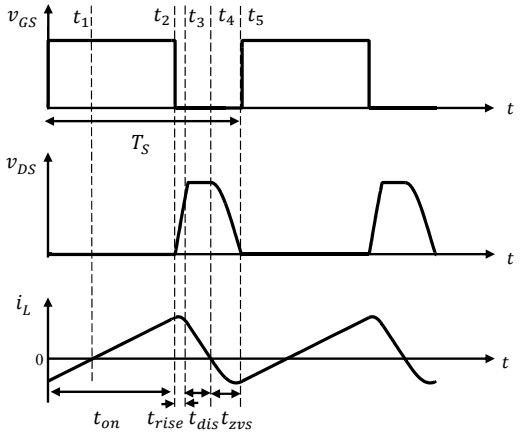

Fig. 4. Key operating wavefors under natural ZVS conditions.

$$t_{zvs} = \frac{1}{\omega_0} arccos\left(\frac{M}{M-1}\right) \tag{11}$$

The only difference respect to the valley switching waveforms, is the fact that the current is still negative when the switching node reaches ZVS conditions. The negative current value can be calculated by using (5) and (11) for $v_{DS}(0) = v_{DS}(t_4) = V_{out}$ and $i_L(0) = i_L(t_4) = 0$ as initial conditions:

$$i_L(t_5) = -\frac{V_{out}}{L\omega_0}\sqrt{1-2M} \tag{12}$$

This negative current changes the initial condition for the current (13) at the switching node rise time t_{rise} that now can be calculated using (13) in (7).

$$i_L(0) = i_L(t_2) = \frac{V_{in}}{L} t_{on} - \left(-i_L(t_5)\right) \tag{13}$$

C. Extended Zero Voltage Switching Operation

If the rectifier diode is replaced with a synchronous rectifier, it is possible to extend the zero voltage switching range of the converter. This can be achieved as previously presented in [23], [24] by extending the conduction time of the rectifier beyond zero current condition in the inductor. The schematic and the converter operating waveforms under extended ZVS conditions are depicted in Fig. 5.

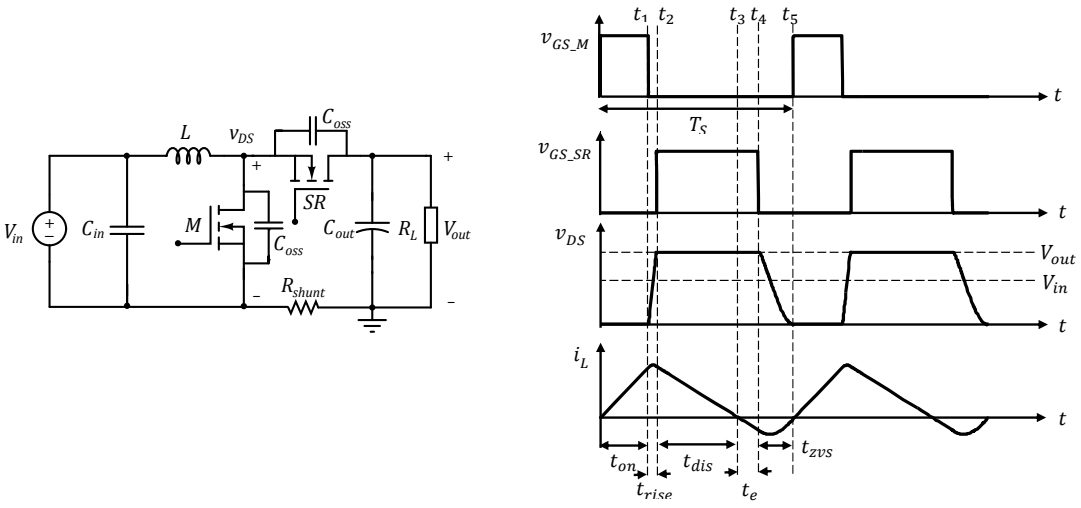

Fig. 5. Conventional boost PFC converter with synchronous rectifier under extended ZVS conditions.

The time to ZVS can be calculated as shown in (14).

$$t_{zvs} = \frac{1}{\omega_0}\left(\pi + arctan\left(\frac{\omega_0 C\left(Mi_L(t_4) + (V_{out} - V_{in})\sqrt{(1-2M)C/L + (i_L(t_4)/V_{out})^2}\right)}{V_{in}(1-M)C/L - i_L(t_4)\sqrt{(1-2M)C/L + (i_L(t_4)/V_{out})^2}}\right)\right) \quad (14)$$

Where the initial current condition and the extra conduction time t_e after zero current condition to achieve ZVS conditions can be calculated by solving for the inductor initial current condition $i_L(0)$ from equations (4) and (5) or in a more graphical way by evaluating the energy transfer in the ideal resonant circuit. Fig. 6 shows the switching node voltage waveform under valley switching conditions and the corrected extended ZVS waveform.

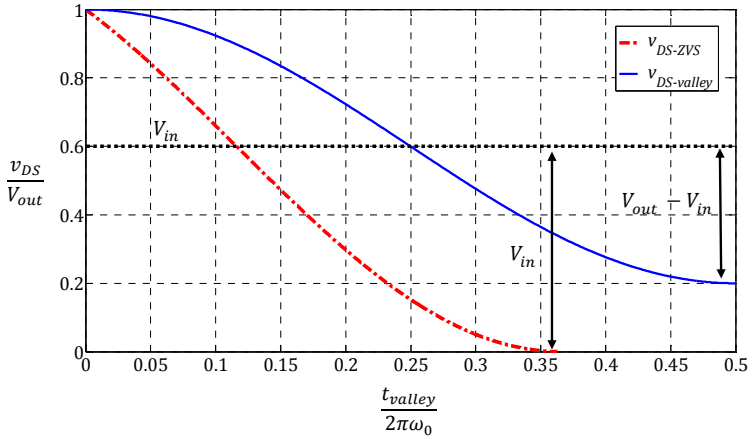

Fig. 6. Switching node voltage waveform under valley switching and extended ZVS conditions.

Initially, under valley switching conditions, all the energy in the resonant circuit is stored in the switching node capacitance. At time instant $1/4 \cdot t_{valley}/2\pi\omega_0$ all the resonant energy in the circuit is stored in the converter input inductor. This energy will be transferred back to the switching node capacitance, producing the switching node voltage to resonate around $V_{in} \pm (V_{out} - V_{in})$. In order to calculate the extra amount of energy that needs to be inserted in to the system to reach ZVS conditions, or to resonate around $V_{in} \pm (V_{in})$ (15) can be used. This expression can be simplified as shown in (16) where $C = 2 \cdot C_{oss}$.

$$\Delta E = \frac{1}{2} \cdot C(V_{in})^2 - \frac{1}{2} \cdot C(V_{out} - V_{in})^2 \quad (15)$$

$$\Delta E = \frac{1}{2} \cdot C \cdot {V_{out}}^2 \cdot (2M - 1) \quad (16)$$

Using (16) it is possible to calculate the input inductor initial current condition, $i_L(0) = i_L(t_4)$ which satisfies ZVS condition at the switching node as shown in (17) and (18). In the same way, the necessary extra conduction time for the synchronous rectifier, can be calculated by using (18) as shown in (19).

$$E_L(t_4) = \frac{1}{2} \cdot i_L(t_4)^2 \cdot L = \frac{1}{2} \cdot C \cdot {V_{out}}^2 \cdot (2M - 1) \tag{17}$$

$$i_L(t_4) = -V_{out} \cdot \sqrt{C/L \cdot (2M - 1)} \tag{18}$$

$$t_e = \frac{-i_L(t_4) \cdot L}{V_{out} \cdot (1 - M)} = \frac{1}{\omega_o} \cdot \frac{\sqrt{2M - 1}}{1 - M} \tag{19}$$

Fig. 7 shows the remaining energy in the switching node capacitor under valley switching operation, and the required initial energy condition in the inductor in order to achieve ZVS normalized to the total energy stored in the switching node capacitance. Fig. 8 presents the normalized synchronous rectifier extra conduction time (t_e), the initial inductor current condition ($i_L(0) = i_L(t_4)$), and the inductor extra charge (ΔQ_L) required for ZVS operation vs. the converter input to output voltage ratio M. All the variables in this figure are controllable quantities by using synchronous rectifier zero current detection in the first case, or by detecting peak current or integrating the current in the other two cases.

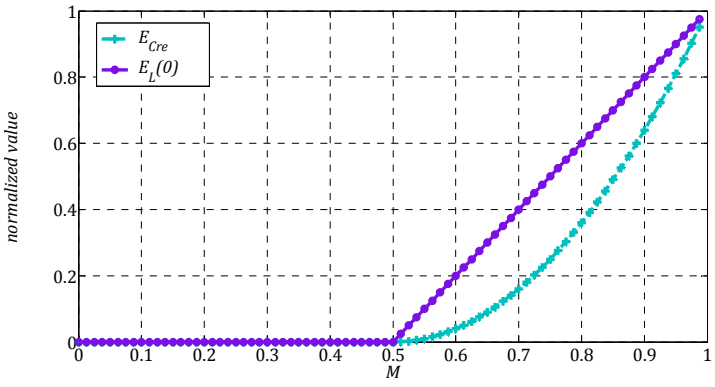

Fig. 7. Remaining stored energy E_{Cre} in the switching node parasitic capacitance under valley switching operation, and initial inductor energy condition $E_L(t_4)$ for ZVS vs. converter input to output voltage ratio M.

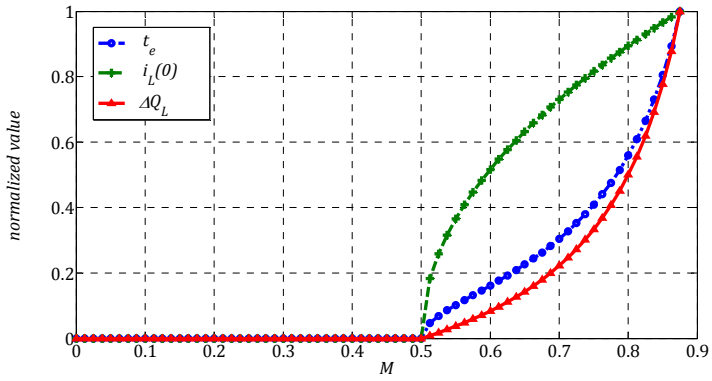

Fig. 8. Extra synchronous rectifier conduction time (t_e), initial inductor current condition ($i_L(t_4)$), and inductor charge increment (ΔQ_L) vs. converter input to output voltage ratio (M).

The work presented in [23] and [24] use the time after zero current detection ($\boldsymbol{t_e}$) as the control variable. A curve fitting based on characterization data is used in order to achieve ZVS based on the converter input and output voltage. However, controlling any of the variable quantities presented in Fig. 8 by using characterization data, requires computational power and more importantly, is sensitive to components tolerance and variations in the propagation delay times. These tolerances, will produce deviations from the approximated values, which will result in failure to achieve ZVS conditions or an increased circulating reactive energy. These situations will lead to an increased capacitive switching loss, or an increased current stress in the converter components resulting in a negative effect on the converter efficiency figures. This work proposes an adaptive ZVS control method based on a control loop which regulates the converter switching node voltage under valley switching conditions by controlling the extra conduction time of the synchronous rectifier t_e. The proposed control method can regulate the switching node voltage to achieve ZVS conditions regardless of components tolerances.

III. ADAPTIVE CONTROL FOR ZVS EXTENSION

This work proposes the implementation of a closed loop control to ensure ZVS conditions under any circumstances. The implemented control loop is based on sampled information from the converter switching node voltage. The control block diagram and the operating waveforms for the proposed solution are shown in Fig. 9 and Fig. 10, respectively. Conventional BCM controllers operating under valley switching conditions, use information of the instantaneous switching node voltage in order to determine the turn-on instant of the main switch, and minimize the energy stored in the parasitic capacitance. In high voltage, and more specifically in PFC applications, this voltage is sensed through an auxiliary winding in the input inductor (W_{aux}). The use of this auxiliary winding makes possible to scale down the switching node voltage, without using resistor divider networks, which are lossy and have bandwidth limitation problems. The proposed control method in this work is similar to a conventional valley switching control scheme, where the derivative of the switching node (v_{DS_der}) is used in order to determine the turn on instant of the main switch. As can be seen in Fig. 9, at t_4 the synchronous rectifier is turned off. After $t_4$the resonant interval t_{zvs} begins, and after the switching node derivative has reached zero volts at t_5, two events take place. First, the scaled down switching node voltage v_{DS_div} obtained from the auxiliary winding voltage($v_{aux} = (v_{DS} - V_{IN}/n)$), is retained in the sampling capacitor $C_{S\&H-1}$. Second, the main switch M is turned on. Turning on the main switch at zero switching node voltage derivative, means the switching node voltage has reached its minimum value, and therefore the main switch can be turned on under minimum switching loss condition. When the main switch M is turned on, the sampled value which is stored in the sampling capacitor $C_{S\&H-1}$ is transferred to the second sampling capacitor $C_{S\&H-2}$. Therefore, the voltage v_{sample} in this sampling capacitor is a continuous voltage waveform representing the switching node voltage under valley switching conditions (or at zero switching node voltage derivative). This sampled voltage is used as the control variable for controlling the extra conduction time t_e of the synchronous rectifier by means of a PI regulator. The implemented control scheme also includes a low speed loop which ensures constant on time of the converter main switch M across the line cycle and regulates the converter output voltage.

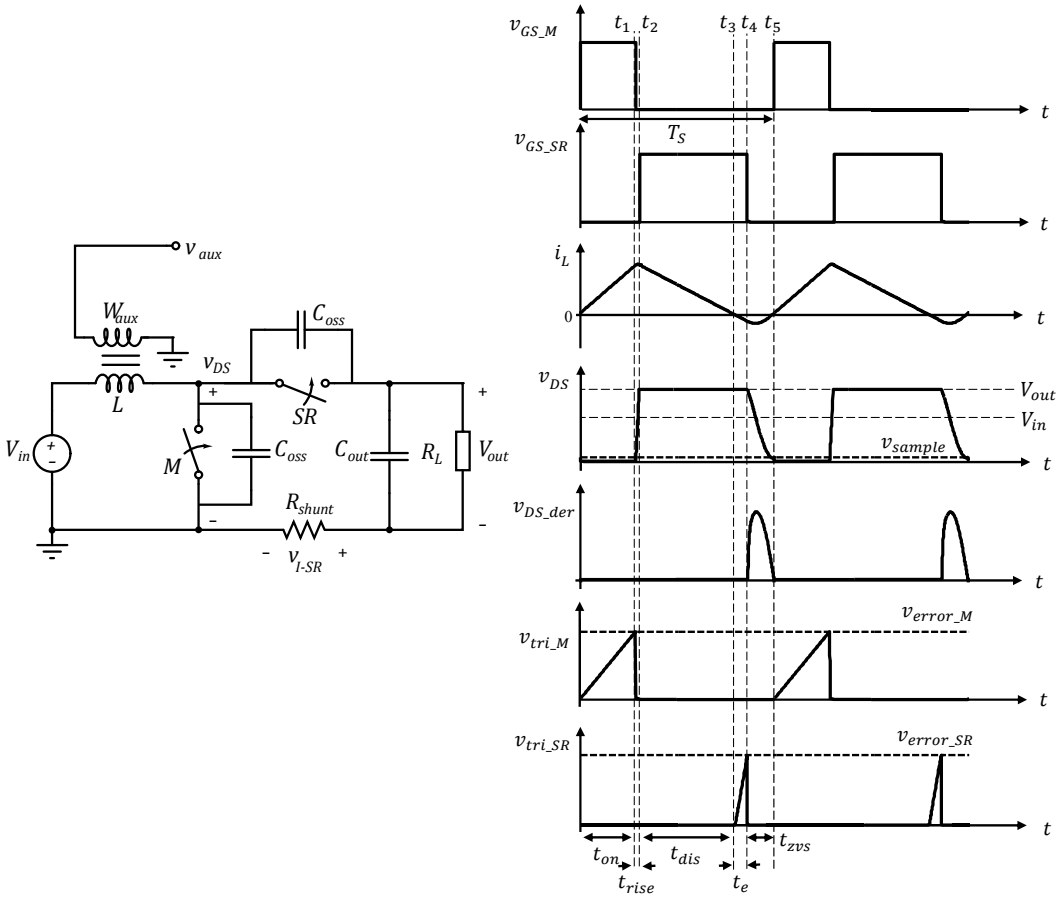

Fig. 9. Proposed ZVS control key waveforms.

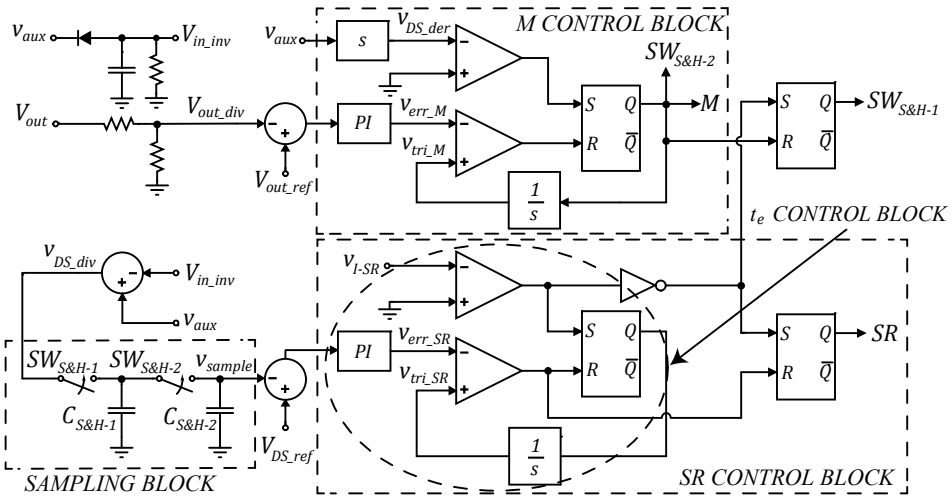

Fig. 10. Proposed ZVS control block diagram.

Fig. 11 shows a Spice based simulation of the implemented control scheme in a conventional boost Power Factor Correction (PFC) converter. The reason for simulating the control on a PFC is to demonstrate the ability of the control loop to regulate the extra conduction time of the synchronous rectifier under a fast changing converter input voltage. In this simulation, the parasitic switching node capacitance is assumed to be ideal. The output capacitance (C_{out}) and load (R_L) are replaced with an ideal voltage source with voltage value V_{out} and the main switch on time (t_{on}) is inserted as a fixed value. Table I shows the values used in this simulation.

TABLE I
SIMULATION PARAMETERS

V_{ac}	230 V_{rms}
V_{out}	400 V
L	100 μH
$C = 2 \cdot C_{oss}$	100 pF
C_{in}	1 μF
$V_{DS}(t_5)$	10 V
k	10 $V/\mu s$
t_{on}	0.8 μs

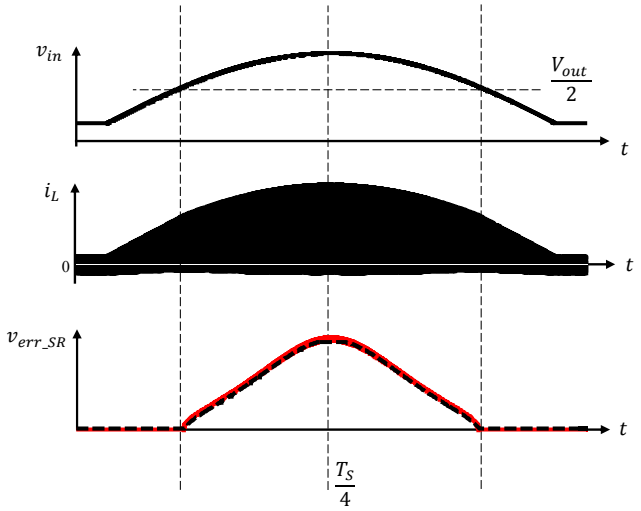

Fig. 11. Simulated error output voltage vs. calculated extra conduction time $\boldsymbol{t_e}$ across half line cycle.

The simulated converter input voltage v_{in} (top waveform), inductor current i_L (middle waveform), and the synchronous rectifier error voltage $v_{error_{SR}}$ (black dotted waveform in the bottom), are plotted across half period of the input line. The reference $V_{DS_{ref}}$ for controlling the switching node voltage is set to regulate the valley switching node voltage to $v_{DS}(t_5) = 10\ V$. Setting a reference slightly higher than zero volts allows error margin for the pi regulator to compensate in both directions without having a significant impact on the capacitive switching loss due to the quadratic relation dependence of the energy with the voltage. The simulated error signal is compared to the calculated extra conduction time t_e using (19), the parameters presented in Table I, and the simulated v_{in} input voltage. The calculated extra conduction time t_e (red waveform in the bottom) is scaled by the gain of the comparator that controls the on time of the synchronous rectifier as in (20). In this simulation the time base for control of the

synchronous rectifier is modeled by an ideal current source and a capacitor with a dv/dt slope of $k = 10V/us$. As can be observed, the control scheme accurately predicts the necessary extra conduction time to operate under ZVS conditions across the input line cycle.

$$v_{error\_SR} = k \cdot t_e = \frac{dv_{tri_{SR}}}{dt} \cdot t_e = 10\ \mathrm{V}/\mu s \cdot t_e \tag{20}$$

A. Controllability of the switching node voltage

This section presents a modelling approach of the controllability of the sampled switching node voltage $v_{sample} = v_{DS}(t_5)$. An accurate model makes it possible to maximize the control loop error suppression and bandwidth. The controllability can be modelled by obtaining the control-to-sampled switching node voltage transfer function $G_v = \hat{v}_{sample}/\hat{v}_{error\_SR}$. Since the extra synchronous rectifier time t_e controls the negative peak inductor current on each cycle, the dynamics of the inductor current will not have any effect on the final switching node voltage. The plant transfer function G_v can be approximated as a gain multiplied by a zero order hold (ZOH) transfer function and a delay time $t_5 - t_4 = t_{ZVS}$ from the moment the extra conduction time is refreshed until the next sample is taken as shown in (21).

$$G_v = \frac{\hat{v}_{sample}}{\hat{v}_{error\_SR}} = k \cdot \frac{\hat{v}_{sample}}{\hat{t}_e} \cdot H_{ZOH}(s) \cdot e^{-st_{zvs}} = \frac{dv_{tri_{SR}}}{dt} \cdot \frac{\hat{v}_{sample}}{\hat{t}_e} \cdot \frac{1 - e^{sT_s}}{sT_s} \cdot e^{-st_{zvs}} \tag{21}$$

Where T_s is the sampling period, which is equal to the converter switching period. The gain $\hat{v}_{sample}/t_e$ can be calculated by particularizing (15) and (17) as in (22) and solving for $v_{DS}(t_5)$.

$$\Delta E = \frac{1}{2} \cdot \frac{(V_{out} - V_{in})^2}{L} \cdot {t_e}^2 = \frac{1}{2} \cdot C\big(V_{in} - v_{DS}(t_5)\big)^2 - \frac{1}{2} \cdot C(V_{out} - V_{in})^2 \tag{22}$$

$$v_{DS}(t_5) = V_{in} - (V_{out} - V_{in})\sqrt{1 + \frac{t_e^2}{LC}} \tag{23}$$

Finally, this gain can be obtained according to [27] by linearizing around the steady state operating conditions by calculating the derivative of (23) respect to t_e as in (24).

$$\begin{aligned} \hat{v}_{sample} &= \frac{\partial v_{DS}(t_5)}{\partial t_e}\hat{t}_e \\ \frac{\hat{v}_{sample}}{\hat{t}_e} &= -\frac{(V_{out} - V_{in})t_e}{\sqrt{1 + \frac{t_e^2}{LC}} \cdot LC} \end{aligned} \tag{24}$$

TABLE II
SIMULATION PARAMETERS

V_{in}	$250\ V$
V_{out}	$400\ V$
L	$100\ \mu H$
$C = 2 \cdot C_{oss}$	$100\ pF$
C_{out}	$10\mu F, 100\ \mu F$
$v_{DS}(t_5)$	$10\ V$
R_L	$1\ k\Omega$
f_s	$485\ k\text{Hz}$

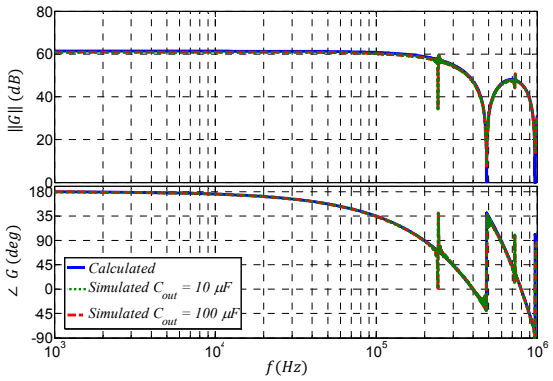

Fig. 12. Simulated vs. calculated control-to-sampled switching node voltage $\hat{v}_{sample}/\hat{v}_{error\_SR}$ transfer function.

Fig. 12 shows the calculated and the simulated $\hat{v}_{sample}/\hat{v}_{error\_SR}$ transfer function for the set of conditions shown in Table II. As it can be observed, the proposed model composed by a gain and a ZOH transfer function with a delay shows very good match with the simulated results.

However, the proposed model, assumes $\hat{v}_{sample}/\hat{v}_{error\_SR}$ perturbation is not affected by the dynamics of the converter output voltage, which is a valid assumption as long as the relation in (25) is fulfilled. Otherwise, the complete transfer function needs to be derived as shown in (26).

$$\frac{\partial v_{ds}(t_5)}{\partial t_e} \gg \frac{\hat{v}_{out}}{\hat{t}_e} \cdot \frac{\hat{v}_{sample}}{\hat{v}_{out}} \tag{25}$$

$$G_v = \frac{\hat{v}_{sample}}{\hat{v}_{error\_SR}} = k \cdot \left(-\frac{(V_{out} - V_{in})t_e}{\sqrt{1 + \frac{t_e^2}{LC}} \cdot LC} + \frac{\hat{v}_{out}}{\hat{t}_e} \cdot \frac{\hat{v}_{sample}}{\hat{v}_{out}} \right) \cdot H_{ZOH}(s) \cdot e^{-st_{zvs}} \tag{26}$$

Where $\hat{v}_{sample}/\hat{v}_{out}$ can be obtained by deriving (23) respect to V_{out} as in (27).

$$\frac{\hat{v}_{sample}}{\hat{v}_{out}} = \sqrt{1 + \frac{t_e^2}{LC}} \tag{27}$$

And where the effect of the extra conduction time on the converter output voltage can be calculated by knowing that the system will behave as a first order system. This is due to the fact that the inductor current is not a state-variable, since the extra conduction time is determined after the zero current detection in each cycle. Therefore, this transfer function can be calculated as the effect of the time perturbation on the average output capacitor and output load current multiplied by their impedances as in (28).

$$\frac{\hat{v}_{out}}{\hat{t}_e} = \frac{\partial I_{C_{out}R_L\_avg}}{\partial t_e} \cdot \frac{R_L}{1 + sC_{out}R_L} \tag{28}$$

Where the average output current circulating through the load and the output capacitor can be derived from Fig. 8 by obtaining the part of the charge of the inductor current that will flow to the output as in (29).

$$I_{C_{out}R_L-avg} = \frac{1}{\mathrm{T}}\left(\int_{t_2}^{t_4} i_L(t)dt + \frac{1}{2}\left(\int_{t_1}^{t_2} i_L(t)dt + \int_{t_4}^{t_5} i_L(t)dt\right)\right) \tag{29}$$

However, as can be seen in Fig. 13, the proposed simplified model with assumption (25) produces accurate results due to large ratio between the equivalent switching node parasitic capacitance and the converter output capacitance. This is due to the fact that the perturbations on the extended conduction time t_e will result in a much larger effect on the sampled switching node voltage than on the converter output voltage. Fig. 13 shows the simulated $\hat{v}_{out}/\hat{v}_{error\_SR}$ and $\hat{v}_{sample}/\hat{v}_{out}$ whose product is at least two orders of magnitude smaller than the error to sample plant transfer function G_v.

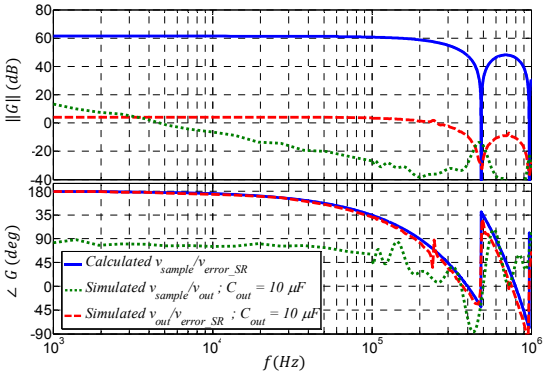

Fig. 13. Simulated control-to-sampled switching node voltage $\hat{v}_{sample}/\hat{v}_{error\_SR}$, output voltage-to-sampled switching node voltage $\hat{v}_{sample}/\hat{v}_{out}$ and control-to-output voltage $\hat{v}_{out}/\hat{v}_{error\_SR}$ transfer functions.

It is also important to notice, on the one hand, that $\hat{v}_{out}/\hat{v}_{error\_SR}$ behaves as a first order system with no inductor dynamics as predicted; and on the other hand, that the simplified model will be valid unless the converter output to switching node capacitance ratio is drastically reduced and the converter operates under light load conditions. Under these situation, $\hat{v}_{out}/\hat{v}_{error\_SR}$ will increase in the low frequency range making assumption (25) not valid anymore.

However, in any case, due to low order and the fast dynamics of the plant transfer function $\hat{v}_{sample}/\hat{v}_{error\_SR}$ is possible to implement a regulation loop capable of regulating the switching node voltage under fast converter operating conditions.

IV. PROTOTYPE IMPLEMENTATION

The proposed control method is implemented using discrete components in a four layer printed circuit board (PCB). The implemented board is designed as a motherboard for the converter power stage. In order to validate the operation under fast input voltage conditions, the implemented prototype is designed as a single phase PFC converter. Fig. 14 shows the implemented ZVS control board. As it can be seen, the implemented control board includes a bridge rectifier and output electrolytic capacitors to test the control in a PFC application. In order to protect the control circuitry, discrete isolated gate drive circuitry is included for both switches. Current mode controllers are used to drive two low inter-winding capacitance transformers to minimize current injection from fast switching node voltage derivatives (dv/dt). Low propagation delay time capacitive couplers are used for gate signal isolation.

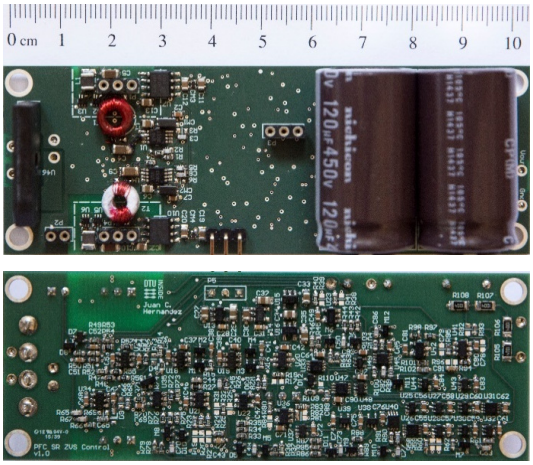

Fig. 14. Top and bottom views of the designed ZVS control PCB.

The converter power stage is implemented using two $600\ V\ 150\ m\Omega$ cascode GaN devices power quad flat no-lead (PQFN) packages for the power semiconductors. A flat current shunt structure as presented in [28],[29],[30] is used for zero current detection purposes. This structure allows to maximize the bandwidth without having a large effect on the loop inductance. A four layer PCB is implemented

where the current loops are minimized to reduce parasitic inductances. Fig. 15 shows the integration of the implemented power stage on the designed control board to minimize the form factor.

Due to the timing requirement in MHz implementations, special care has been taken to minimize propagation delay times through the control circuitry. However, the most critical aspect of the implementation of the proposed control method is the sample and hold circuitry that feeds the reconstructed switching node voltage $v_{DS}(t_5)$ to the error amplifier that regulates the synchronous rectifier extra conduction time. The switching node voltage is reconstructed from the auxiliary winding as shown in Fig. 9. The reconstruction of the voltage v_{DS_div} and the sampling cells are implemented using 345 MHz $LMH6611$ operational amplifiers. The operational amplifier output voltages are limited and the gains kept equal to one to achieve the circuit bandwidth requirement. The sample and hold cell is implemented using 30 V fast NMOS switches $NX3020NAK$ to maximize speed and minimize charge injection into the sampling capacitor.

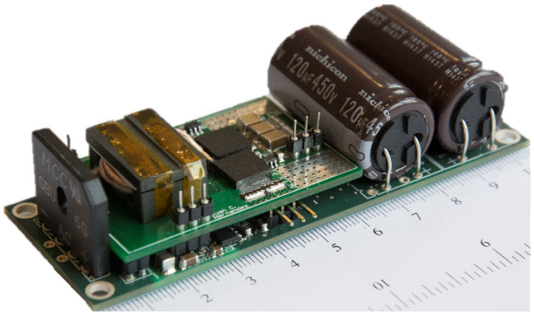

Fig. 15. Integration of the proposed ZVS control and power stage PCBs.

Fig. 16 shows the converter operating waveforms under extended ZVS operation for $v_{in} =$ 75 V and $v_{out} = 110\ V$. The reference for regulating the switching node voltage under valley switching conditions is adjusted to produce $v_{DS}(t_5) = 10\ V$. The bottom trace shows the voltage in the first sample and hold cell capacitor $v_{C_{S\&H-1}}$. When the synchronous rectifier is turned on, the first sample and hold switch is turned on and the sampling capacitor voltage is equal to the reconstructed switching node voltage. When the converter switching node derivative reaches zero after the synchronous rectifier is turned off,

the first sampling cell will retain the sampled voltage until the next switching cycle. As it can be observed, after the inductor current reaches zero, the implemented control scheme extends the synchronous rectifier conduction time to regulate the switching node voltage based on the stored sample.

Fig. 17 shows the measured control-to-sample plant transfer function $\hat{v}_{sample}/\hat{v}_{error\_SR}$ under the conditions depicted in Fig. 16. As it can be observed the plant transfer function behaves accordingly to the proposed gain with ZOH model. Fig. 18 shows the converter operating under a 50 Hz input ac voltage. It can be observed the extra conduction time error amplifier signal v_{error_SR} in phase with the converter input voltage, which demonstrates the ability of the control to respond to fast changing converter input voltage conditions.

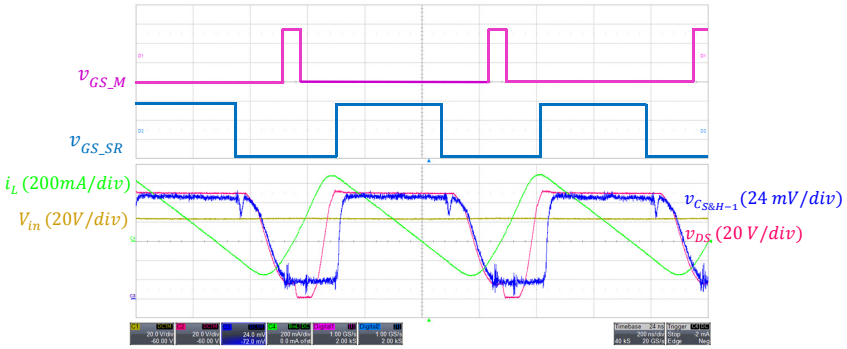

Fig. 16. Converter operating waveforms under extended ZVS operation. Top digital channels: main switch gate signal v_{GS_M} and synchronous rectifier gate signal v_{GS_SR}. Bottom analog channels: converter input voltage V_{in} ($20V/div$), converter switching node voltage v_{DS} ($20V/div$), first sample and hold cell capacitor voltage $v_{C_{S\&H-1}}$ (24 mV/div), and inductor current i_L (200 mA/div). Time scale 200 ns/div.

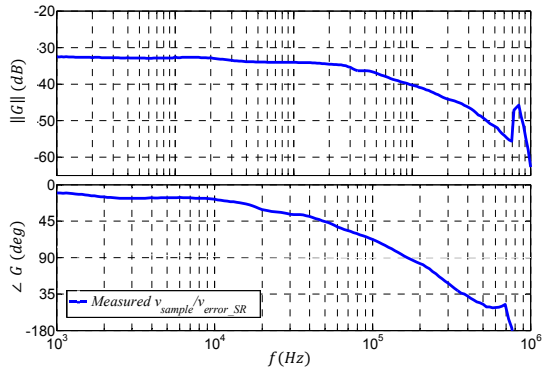

Fig. 17. Measured control-to-sampled switching node voltage $\hat{v}_{sample}/\hat{v}_{error\_SR}$ transfer function.

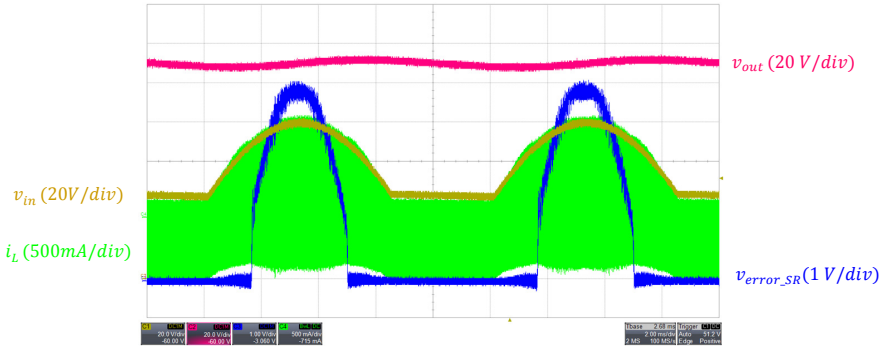

Fig. 18. Converter operating waveforms across one line cycle. Converter input voltage v_{in} (20V/div), output voltage v_{out} (20V/div), inductor current i_L (500mA/div) and error amplifier control signal v_{error_SR} (1V/div). Time scale 2 ms/div.

V. CONCLUSION

BCM or CrM mode implementations are gaining popularity due to the integration of wide band-gap GaN semiconductors. Various GaN based BCM converters have been reported in the literature operating in the MHz switching frequency range. It is proven that the increased current stress in BCM implementations using GaN devices is compensated by the reduction in switching losses at the main switch turn on event due to ZCS and ZVS or valley switching conditions. However, the ability of the converter to operate under ZVS conditions, or the amount of energy recovered under valley switching conditions, is determined by the switching node capacitance and the converter input to output voltage ratio M. On the other hand, extension of the ZVS range is possible in implementations using synchronous rectification, which is achieved by extending the synchronous rectifier conduction time after zero current condition at the inductor. This operation mode enables high efficiency MHz implementations independently of the converter operating conditions. However, no previous research has addressed an adaptive control method for this operating mode. As discussed before, previously proposed solutions are based on experimental characterization data making this operation mode non feasible due to component tolerances and variations in the propagation delay times. This work presents and validates an adaptive control method capable of regulating the synchronous rectifier conduction time based on a regulation loop of the switching node conditions. The proposed method is validated through simulation and experimental results. Moreover, a model is derived to analyze the controllability of the switching node voltage

switching conditions. The proposed model is verified and proves the feasibility of the proposed control method to achieve ZVS under fast perturbations of the converter operating conditions.

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Isolated Boost Converter with Bidirectional Operation for Supercapacitor Applications

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Isolated Boost Converter with Bidirectional Operation for Supercapacitor Applications

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Abstract

This paper presents an isolated bidirectional dc/dc converter based on primary parallel isolated boost converter (PPIBC). This topology is an efficient solution in low voltage high power applications due to its ability to handle high currents in the low voltage side. In this paper, the converter has been modeled using non-ideal components and operated without any additional circuitry for startup using a digital soft-start procedure. Simulated and measured loop gains have been compared for the validity of the model. On-the-fly current direction change has been achieved with a prototype interconnecting two battery banks. A second prototype has been constructed and tested for supercapacitor operation in constant power charge mode.

Key words: Battery, Bidirectional, Isolated, Modeling, Startup, Supercapacitor

NOMENCLATURE

$R_{D_{Bat}}$	Battery dynamic resistance
$V_{OC_{Bat}}$	Battery open circuit voltage
R_{ESR}	Supercapacitor series resistance
V_{SC}	Supercapacitor voltage
r_L	Inductor parasitic resistance
$r_{M\,P}$	Primary MOSFETs on resistance
r_p	Transformer primary resistance
r_S	Transformer secondary resistance
$r_{M\,S}$	Secondary MOSFETs on resistance
r_{ESR}	Capacitor series resistance

I. INTRODUCTION

Nowadays the depletion of fossil fuels together with the awareness of the climate change is forcing the industry to move towards green energy solutions. The same change is starting to be a reality in transportation industry where hybrid and electric vehicles are presented as an alternative solution to CO2 emission reduction. Extension of the driving range in electric vehicles has become one of the main concerns to make this an attractive technology. Special efforts have been taken to improve the capacity of the energy storage elements and to increase the efficiency of all the parts inside the power drive train. Regenerative brakin g is one of the adopted solutions for increasing the driving range by recovering the kinetic energy of the vehicle during the braking process.

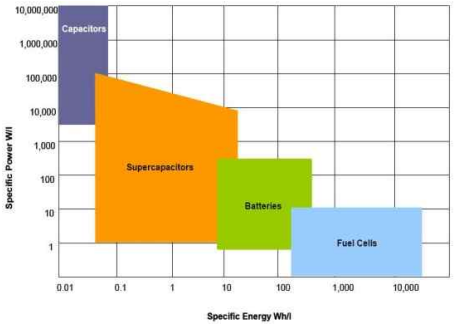

Fig. 1. Ragone chart. Power density vs. energy density for various energy storage systems [1].

Supercapacitors have relatively large power density, as shown in Fig. 1, and are the preferred energy storage elements in regenerative braking applications. The aim of this work is to integrate a supercapacitor bank in a fuel cell powered drive train (Fig. 2) to increase the dynamics and the power density of the system.

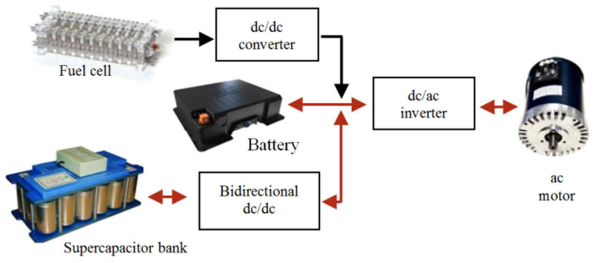

Fig. 2. Supercapacitor and bidirectional converter integration into a fuel cell powered drive train.

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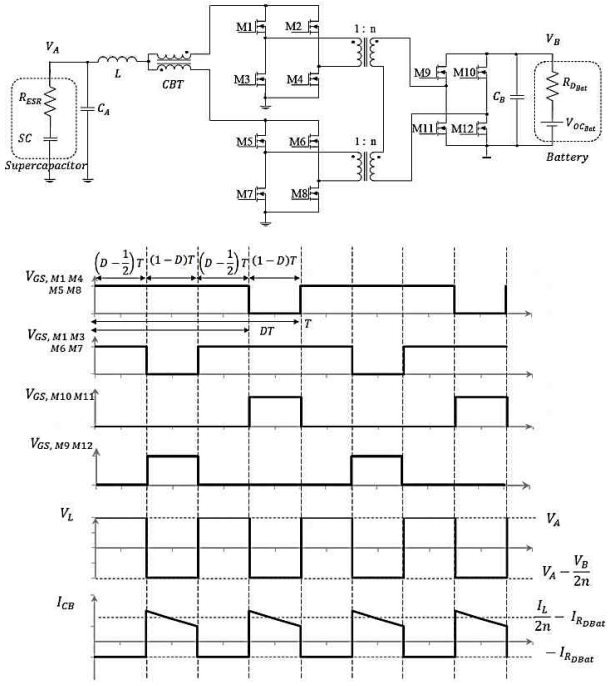

Fig. 3. Converter schematic (up) and boost mode steady state operating waveforms (down).

Different bidirectional dc-dc converter topologies have been proposed and investigated in the literature so far [2]-[7]. PPIBC is an efficient solution for low voltage high current applications [8]-[9]. Due to the transformer series connection on the secondary side, the current on each parallel primary stage is forced to be equal. However, different stray inductances in the current path or mismatches in the gate drive signal can cause the input current of each full bridge deviate from each other. In order to prevent this situation a current balancing transformer (CBT) is inserted to the circuit in series with the input inductor [10]. The CBT, which is implemented as an inverse coupled inductor, shows high impedance between the two parallel primary stages and keeps the branch currents to be equal. The schematic and waveforms of the proposed bidirectional converter are shown in Fig. 3.

In this topology, parallel primary power stages share the same control signals with the same phase switching sequence for the corresponding switches, which allows a simple control, similar to a simple isolated boost converter.

Output rectification unit as well as input and output filters are common to both of the parallel primary stages. The paralleling method splits the critical high ac-current-loop into two smaller loops. Each of the smaller loops only needs to switch half of the input current thereby achieving higher conversion efficiency. Since the two transformers share the same input current and have their secondary windings connected in series, a higher turns-ratio transformer can be replaced by two lower turns-ratio transformers, which allows a simple design and manufacturing of the transformers.

In this paper bidirectional operation of the PPIBC is studied. An accurate dynamic model of the converter has been derived taking into consideration the component non-idealities. Simple supercapacitor and battery models with internal impedances are also included in the model. PPIBC has been reduced to a simple boost converter in order to derive the state space equations.

Gain and phase plots of the compensated loop have been obtained from both the derived model and the experimental setup.

II. CONVERTER MODELING

Due to the large voltage time constant of batteries and supercapacitors, for small signal modeling purposes, these components can be treated as ideal voltage sources with an equivalent series resistance. Dc-dc converters interfacing this kind of energy storage elements need to be designed based on an accurate small signal model. This is due to the fact that the low value of the supercapacitor and battery series resistance makes the current flow in the converter to be very sensitive to duty cycle perturbations [11].

State space average modeling has been used to obtain an accurate model that predicts the dynamics of the system in a precise way. The converter parasitic resistances have been included in the model since they are in the same range with the battery and supercapacitor series resistances. Consequently, not considering these parasitics will have an effect on the dc gain of the plant transfer functions.

Fig. 4 shows the first state of the converter that corresponds to the charging state in boost mode and the discharging state in buck mode. Fig. 5 shows the simplified version of Fig. 4 where the two transformers are combined into an equivalent transformer with a turn ratio of 1: 2n. All the components are reflected to the inductor side and parasitic resistances are combined into an equivalent resistance $(r_{eq\,1})$.

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_{C_A}(t) \\ v_{C_B}(t) \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}\cdot\left(r_{eq\,1} + \frac{r_{esrA}\cdot R_{ESR}}{R_{ESR}+r_{esrA}}\right) & \frac{R_{ESR}}{L\cdot(R_{ESR}+r_{esrA})} & 0 \\ -\frac{R_{ESR}}{C_A\cdot(R_{ESR}+r_{esrA})} & -\frac{1}{C_A\cdot(R_{ESR}+r_{esrA})} & 0 \\ 0 & 0 & -\frac{1}{C_B\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} \end{bmatrix}\cdot\begin{bmatrix} i_L(t) \\ v_{C_A}(t) \\ v_{C_B}(t) \end{bmatrix} + \begin{bmatrix} \frac{r_{esrA}}{L\cdot(R_{ESR}+r_{esrA})} & 0 \\ \frac{1}{C_A\cdot(R_{ESR}+r_{esrA})} & 0 \\ 0 & \frac{1}{2\cdot C_B\cdot n\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} \end{bmatrix}\cdot\begin{bmatrix} V_{SC} \\ V_{OC_{Bat}} \end{bmatrix} \quad (5)$$

$$V_B(t) = \begin{bmatrix} 0 & 0 & \frac{R_{D_{Bat}}}{R_{D_{Bat}}+r_{esrB}} \end{bmatrix}\cdot\begin{bmatrix} i_L(t) \\ v_{C_A}(t) \\ v_{C_B}(t) \end{bmatrix} + \begin{bmatrix} 0 & \frac{r_{esrB}}{2\cdot n\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} \end{bmatrix}\cdot\begin{bmatrix} V_{SC} \\ V_{OC_{Bat}} \end{bmatrix} \quad (6)$$

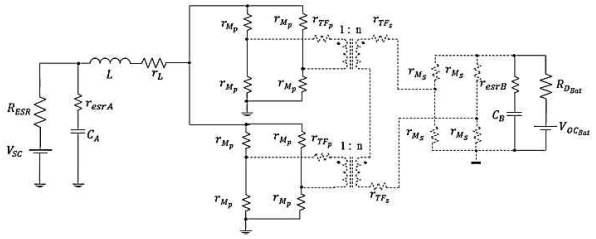

Fig. 4. Converter first state with parasitic resistances.

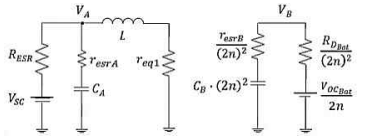

Fig. 5. Simplified equivalent circuit. Converter first state.

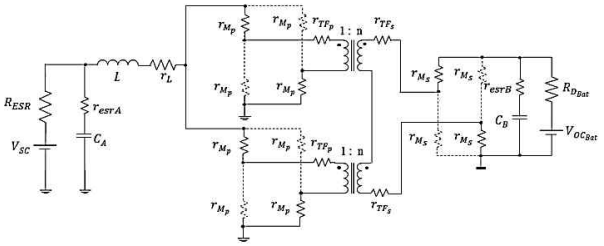

Fig. 6. Converter second state with parasitic resistances.

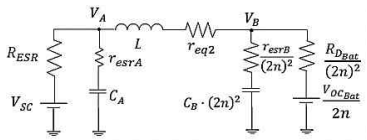

Fig. 7. Simplified equivalent circuit. Converter second state.

Fig. 6 presents the second state of operation corresponding to the discharging state of the boost mode and the charging state of the buck mode. Similar to the previous state the circuit is reduced to a simpler form as shown in Fig. 7.

The equivalent resistances in Fig. 5 and Fig. 7 are given by (1) and (2).

$$r_{eq1} = r_L + r_{MP}/2 \tag{1}$$

$$r_{eq2} = r_L + r_{MP} + \frac{r_P}{2} + \frac{2r_S}{(2n)^2} + \frac{2r_{MS}}{(2n)^2} \tag{2}$$

Based on the simplified circuits for both operating states, the state and output matrixes can be written in the form of (3) and (4) as in (5) and (6) for the first converter state.

$$\frac{dx(t)}{dt} = A_1 x(t) + B_1 u(t) \tag{3}$$

$$V_B(t) = q_1 x(t) + k_1 u(t) \tag{4}$$

In the same way, (7) and (8) can be obtained as shown in (9) and (10) for the second converter state.

$$\frac{dx(t)}{dt} = A_2 x(t) + B_2 u(t) \tag{7}$$

$$V_B(t) = q_2 x(t) + k_2 u(t) \tag{8}$$

The state, input and output matrixes are obtained by averaging the individual matrixes for each state over a period as shown in (11), (12), (13) and (14).

$$A = A_1 \cdot d + A_2 \cdot (1-d) \tag{11}$$

$$B = B_1 \cdot d + B_2 \cdot (1-d) \tag{12}$$

$$q = q_1 \cdot d + q_2 \cdot (1-d) \tag{13}$$

$$k = k_1 \cdot d + k_2 \cdot (1-d) \tag{14}$$

After perturbing the circuit around a steady state operating point, the first order terms are collected to obtain the linear model as in (15) and (16).

$$\hat{x} = A \cdot \hat{x} + B \cdot \hat{u} + [(A_1 - A_2)X + (B_1 - B_2) \cdot U] \cdot \hat{d} \tag{15}$$

$$\hat{v}_b = q \cdot \hat{x} + k \cdot \hat{u} + [(q_1 - q_2)X + (k_1 - k_2) \cdot U] \cdot \hat{d} \tag{16}$$

The term X corresponds to the steady state solution given in (17).

$$X = -A^{-1} \cdot B \cdot U \tag{17}$$

Finally the small signal expressions of the state variables and the high side output voltage can be obtained by making $\hat{u}$ equal to zero and applying the Laplace transformation to (15) and (16) obtaining (18) and (19) respectively.

$$\hat{x} = (sI - A)^{-1} \cdot [(A_1 - A_2)X + (B_1 - B_2)U] \cdot \hat{d} \tag{18}$$

$$\hat{v}_b = \left[q \cdot (sI - A)^{-1} \cdot [(A_1 - A_2)X + (B_1 - B_2)U]\right] \cdot \left[+[(q_1 - q_2)X + (k_1 - k_2) \cdot U]\right] \cdot \hat{d} \tag{19}$$

The derived equations are valid independent of the power flow direction because the same differential equations govern the circuit for buck and boost operation modes. For this reason a single model is derived for both operating modes. In other words, if we consider the boost operating mode, the inductor charging subinterval is defined as dT which corresponds to discharging subinterval for buck mode defined

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_{C_A}(t) \\ v_{C_B}(t) \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}\cdot\left(r_{eq2} + \frac{r_{esrB}\cdot R_{D_{Bat}}}{4\cdot n^2\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} + \frac{r_{esrA}\cdot R_{ESR}}{R_{ESR}+r_{esrA}}\right) & \frac{R_{ESR}}{L\cdot(R_{ESR}+r_{esrA})} & -\frac{R_{D_{Bat}}}{L\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} \\ -\frac{R_{ESR}}{C_A\cdot(R_{ESR}+r_{esrA})} & -\frac{1}{C_A\cdot(R_{ESR}+r_{esrA})} & 0 \\ \frac{R_{D_{Bat}}}{4\cdot C_B\cdot n^2\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} & 0 & -\frac{1}{C_B\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} \end{bmatrix} \cdot \begin{bmatrix} i_L(t) \\ v_{C_A}(t) \\ v_{C_B}(t) \end{bmatrix} + \begin{bmatrix} \frac{r_{esrA}}{L\cdot(R_{ESR}+r_{esrA})} & -\frac{r_{esrB}}{2\cdot n\cdot L\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} \\ \frac{1}{C_A\cdot(R_{ESR}+r_{esrA})} & 0 \\ 0 & \frac{1}{2\cdot n\cdot C_B\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} \end{bmatrix} \cdot \begin{bmatrix} V_{SC} \\ V_{OC_{BatB}} \end{bmatrix} \tag{9}$$

$$V_B(t) = \begin{bmatrix} \frac{R_{D_{Bat}}\cdot r_{esrB}}{4\cdot n^2\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} & 0 & \frac{R_{D_{Bat}}}{R_{D_{Bat}}+r_{esrB}} \end{bmatrix} \cdot \begin{bmatrix} i_L(t) \\ v_{C_A}(t) \\ v_{C_B}(t) \end{bmatrix} + \begin{bmatrix} 0 & \frac{r_{esrB}}{2\cdot n\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} \end{bmatrix} \cdot \begin{bmatrix} V_{SC} \\ V_{OC_{Bat}} \end{bmatrix} \tag{10}$$

TABLE I

CONVERTER OPERATION MODES

Boost Mode		Buck Mode
d	=	$1-d$
$1-d$	=	d
A_1	=	A_2
A_2	=	A_1
B_1	=	B_2
B_2	=	B_1
A	=	A
B	=	B

as $(1-d)T$. This duality is valid for all the converter dynamic expressions between buck and boost operating modes. Consequently, the final state equations remain the same independent of the power flow direction as shown in Table I.

III. CONTROL STRATEGY

In this application, current control on the battery side is preferred in order to absorb and deliver the necessary current to the inverter during regenerative braking and acceleration events. In this operation mode the supercapacitor is charged and discharged with constant power between the nominal voltage and half the nominal voltage to avoid high current stress on the low voltage side. However, when the supercapacitor voltage is under half of the nominal value due to the effect of leakage currents during long periods of inactivity of the system, the supercapacitor will be charged with constant current by controlling the inductor current.

From the state variable solution (18), the duty cycle-to-inductor current transfer function is obtained. Moreover, the duty cycle-to-high side output current can be obtained by dividing the duty cycle-to-high side voltage transfer function (19) by the battery dynamic resistance as shown in (20).

$$G_{IB}(s) = \left.\frac{\hat{\imath}_B(s)}{\hat{d}(s)}\right|_{\hat{u}=0} = \frac{G_{VB}(s)}{R_{dbat}} \tag{20}$$

LTspice IV simulations are performed to validate the derived model by comparing the gain and phase plots. The steady state value of the inductor current is selected to be 100A in both power flow directions. The converter duty cycle is calculated from the dc steady state solution given in (17). The selected parameters for the simulations are presented in Table I.

Fig. 8 and Fig. 9 present the calculated and simulated gain and phase plots of the converter duty cycle-to-inductor current transfer function in boost and buck operation modes respectively. Very close matching between the simulation and the calculated model is achieved. It can be observed that the obtained plant transfer function is very similar for both modes. Only a small difference in the low frequency gain between the two operating modes can be observed. This effect is produced by the voltage drop across the parasitic resistances of the system.

TABLE II

CONVERTER SIMULATION PARAMETERS

L	5 μH
r_L	1 $m\Omega$
I_L	100 A
n	1/2
V_{SC}	30 V
R_{ESR}	10 $m\Omega$
$V_{OC_{Bat}}$	80 V
$R_{D_{Bat}}$	40 $m\Omega$
r_{MP}	10 $m\Omega$
r_p	5 $m\Omega$
r_{MS}	5 $m\Omega$
C_A	100 μF
r_{esrA}	2 $m\Omega$
C_B	200 μF
r_{esrB}	1 $m\Omega$

Fig. 10 and Fig. 11 show the comparison between the calculated and simulated duty cycle-to-high side output current transfer function. Equal than before very close matching between the simulation and the calculation is achieved. In this case, the dynamics of the system depend on the current flow direction because of the presence of a right half plane zero in boost operation mode.

IV. EXPERIMENTAL RESULTS

The first PPIBC prototype is shown in Fig. 12. The converter is controlled by using a 32 bit fixed point DSP.

The two transformers are integrated into the same magnetic core structure. This integrated magnetic component is constructed with four halves of ELP64/10/50 based on N87 core material.

The input inductor is built using four halves of E64/10/50 based on 3F3 material. The windings in both magnetic components are implemented using PCB boards with FR4 material. The inductor current is sensed by a Hall Effect current transducer LAS100-TP. The current measurement is low pass filtered by a differential amplifier to avoid aliasing at the ADC input.

In order to test the bidirectional operation, the prototype is connected to two battery banks at the low and high voltage side. The battery bank on the low voltage side is formed by three series connected AGM batteries Haze HZB-EV12-26

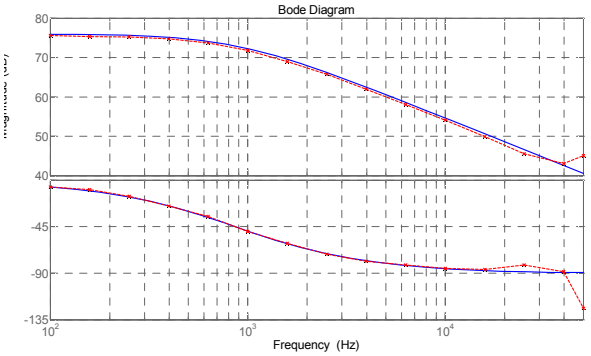

Fig. 8. Duty cycle-to-inductor current boost mode. Calculated (blue) and simulated (red).

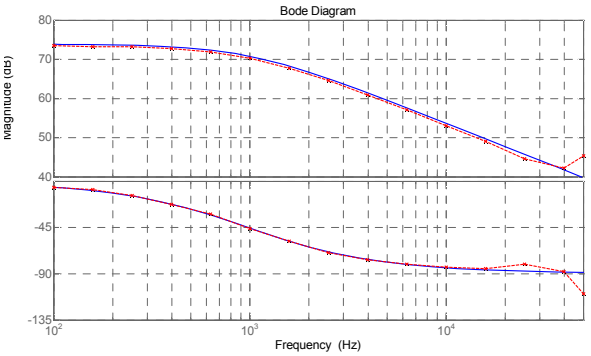

Fig. 9. Duty cycle-to-inductor current buck mode. Calculated (blue) and simulated (red).

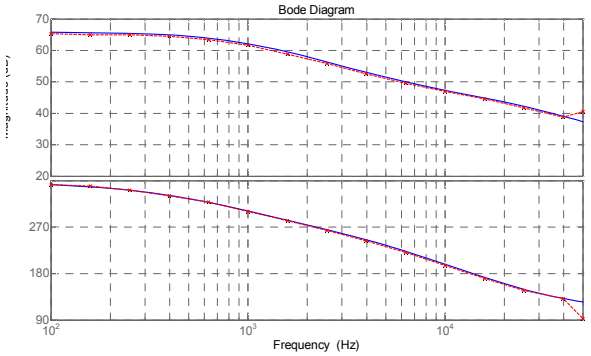

Fig. 10. Duty cycle-to-output current boost mode. Calculated (blue) and simulated (red).

which are rated for 12 volts and 26 Ah. On the high voltage side, the battery bank is composed of four series connected batteries of the same type. In this prototype, the inductor current is the selected control variable.

The battery impedance is measured and the obtained value at 1 kHz is used in the derived dynamic model to match the gain at the desired converter crossover frequency. The converter parameters are shown in Table III and the parasitic resistances are presented in Table IV. The magnetic component parasitic resistances correspond to the measured values at 1 kHz.

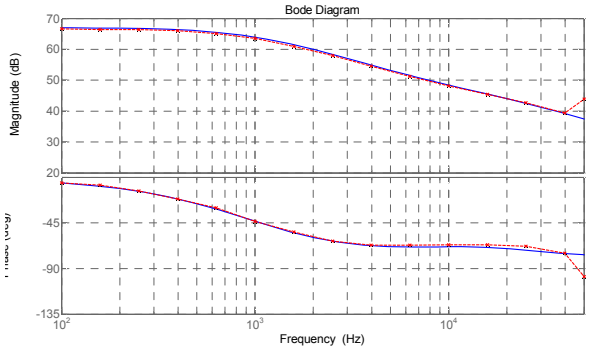

Fig. 11. Duty cycle to-output-current buck mode. Calculated (blue) and simulated (red).

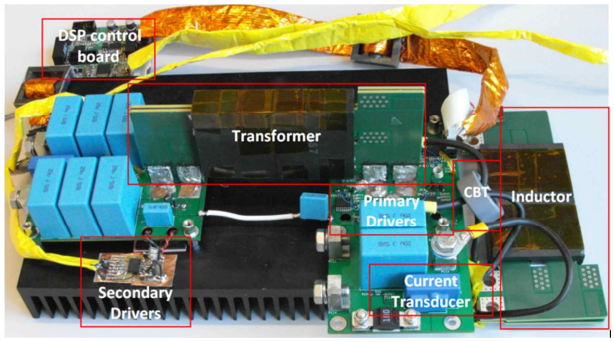

Fig. 12. First PPIBC prototype.

It is important to note that for calculating the dc operating point, the battery terminal voltage will change as a function of the current direction and magnitude as well as the battery state of charge (SOC). As presented in [12], the battery can be modeled as a dependent voltage source in series with the battery dynamic resistance. True understanding of the changes in the terminal voltages is possible through accurate modeling of the battery with capacitance-like effects of the battery internal chemistry, which is beyond the scope of this work.

In this paper the battery terminal voltages are measured at the desired operating conditions as shown in Table V. These values are used in the model to calculate the converter dc operating point.

The converter loop measurements are performed for both operating modes with a dc power supply as the input source to the converter and the corresponding battery bank as the converter load. The power supply output resistance is assumed to be negligible at the frequencies of interest. Moreover, it should to be noticed that the measured battery terminal voltages already include the voltage drop across the battery dynamic resistances.

The converter inductor current control loops are compensated by inserting an integrator and a zero before the lower frequency pole of the plant transfer function. Although

TABLE III

PARAMETERS OF THE CONVERTER

Battery A open circuit Voltage	$36V$
Battery B open circuit Voltage	$48V$
Transformer turn ratio	$1:3$
Inductor	$13.5\ \mu H$
Transformer and inductor core material	Ferrite 3F3
Capacitor A	$40\ \mu H$
Capacitor B	$120\ \mu H$
Switches M1-M8	IPA075N15N3 G
Switches M9-M12	FDH055N15A
Switching frequency	$50\ kHz$
Battery A dynamic resistance	$60\ m\Omega$ @ 1kHz
Battery B dynamic resistance	$80\ m\Omega$ @ 1kHz

TABLE IV

CONVERTER PARASITIC RESISTANCES

r_L	$3.9\ m\Omega$
r_{MP}	$7.5\ m\Omega$
r_p	$3.5\ m\Omega$
r_S	$0.4\ m\Omega$
r_{MS}	$5.9\ m\Omega$
r_{esrA}	$3.15\ m\Omega$
r_{esrB}	$1.1\ m\Omega$

TABLE V

CONVERTER STEADY OPERATING CONDITIONS

Boost Mode	Buck Mode
$V_G = 33.6\ V$	$V_{BatA} = 41\ V$
$V_{BatB} = 56.1\ V$	$V_G = 48\ V$
$I_L = 10\ A$	$I_L = -10\ A$
$d = 0.604$	$d = 0.422$

the converter plant transfer function is the same regardless of the current direction, different controllers have been used for boost and buck operation modes. This is due to the fact that the converter dc operating point is changed due to the battery terminal voltage being dependent on the current direction, which affects the converter transfer function. The compensation gain has been adjusted for a loop crossover frequency of 1 kHz for both operating modes.

Fig. 13 presents a measurement of the converter steady state waveforms. Fig. 14 and Fig. 15 show the calculated and

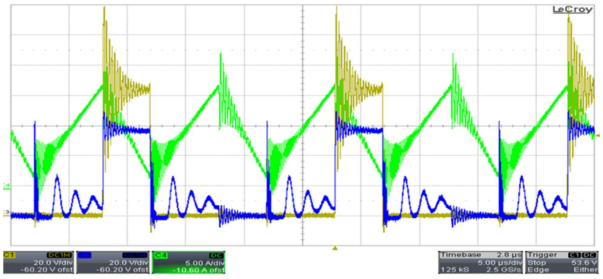

Fig. 13. Inductor current (green, 5A/div) with low voltage side (light brown, 20V/div) and high voltage side (blue, 20V/div) drain to source voltage waveforms during steady state operation. Time scale: 5μs/div.

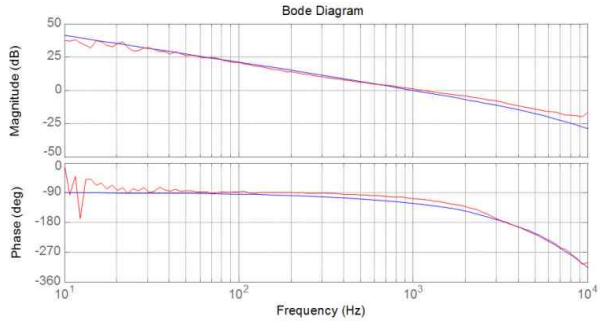

Fig. 14. Calculated (blue trace) and measured (red trace) open loop transfer function boost mode.

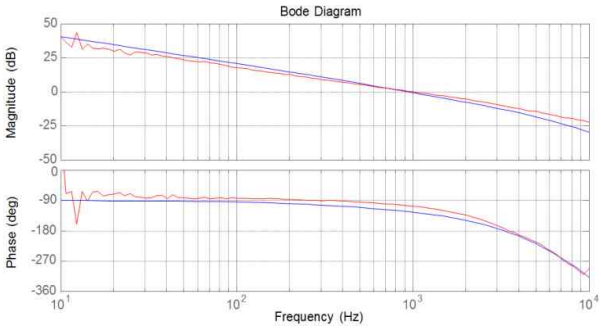

Fig. 15. Calculated (blue trace) and measured (red trace) open loop transfer function buck mode.

measured converter loop gain and phase plots where close matching can be observed. The calculated model includes the controller transfer function implemented inside the DSP with the sampling, calculation and PWM reconstruction delays, as well as the signal conditioning amplifier transfer function.

After designing the controllers for both operation modes, a soft start procedure of the converter needs to be implemented.

The implemented soft start function is able to turn on the converter in both directions without any additional circuitry.

While working with batteries, the duty cycle to inductor current transfer function has a larger gain compared to a pure resistive load for the same power level, meaning that the inductor current is very sensitive to small duty cycle perturbations in case of battery applications [11]. The converter has to be started with minimum duty cycle without

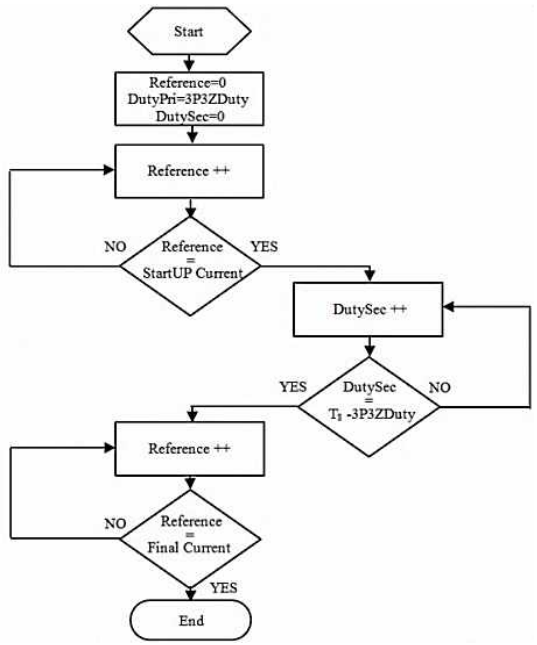

Fig. 16. Converter soft start flow diagram.

using synchronous rectification. Otherwise, starting with minimum duty cycle on one side will correspond to maximum duty cycle to the other side, creating an uncontrolled amount of initial current flow in the incorrect direction during converter startup. To avoid this situation, the converter should first be started by raising the current reference up to a certain startup current level. This current level has to be big enough to ensure CCM operation of the converter; otherwise, if the synchronous rectification is initiated, the duty cycle-to-inductor current transfer function will present a difference in dynamic behavior between DCM and CCM operation, resulting in an uncontrolled current increase until the control loop manages to compensate the error. Once the current trough the inductor has reached the desired level which ensures CCM operation, synchronous rectification can be started. At this point, the duty cycle for the synchronous MOSFETs is increased very slowly from zero to the final value calculated by the control law. This progressive introduction of the synchronous rectification avoids the current level to change again because of the difference in conduction resistance between the MOSFETs and the body diodes (used during normal rectification) that will affect the converter steady state conditions.

Once the synchronous rectification has been introduced, the final step is to increase the reference value up to the desired final current level. This soft start procedure removes unnecessary current and voltage stress from the switches at the start up increasing the converter reliability. The flow diagram of the proposed soft start procedure is presented in Fig. 16.

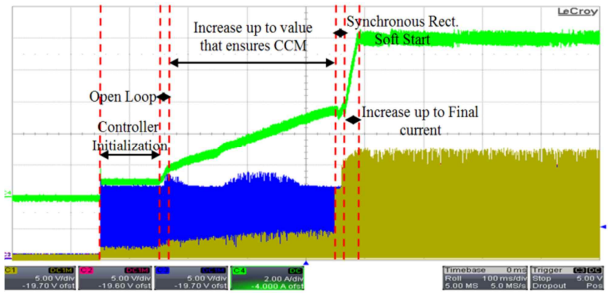

Fig. 17. Converter gradual soft start with two level inductor current reference change (green, 2A/div). Low voltage side MOSFETs gate waveform (blue, 5V/div) and high voltage side MOSFETs gate waveform (light brown, 5V/div.)Time scale: 100ms/div.

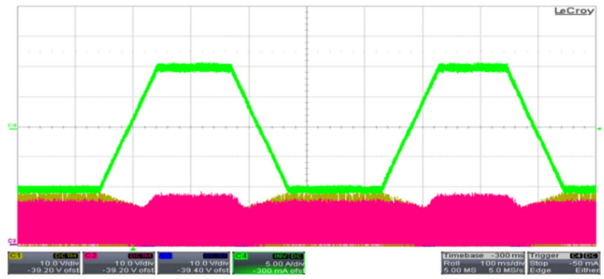

Fig. 18. Inductor current direction change with a defined ramp (5A/div. Time scale: 100ms/div).

Fig. 17 shows the detailed startup sequence where the converter input current on the low voltage side together with the gate waveforms of the MOSFETs can be observed. Fig. 18 shows the bidirectional operation of the converter with average inductor current control. The figure shows four current direction change events where the current change transition time has been adjusted to 100 ms.

After testing the soft start procedure and the bidirectional operation of the converter, a second PPIBC prototype with an input power of 8kW is constructed. This converter is used for testing operation with a supercapacitor module with constant power charge by controlling the high side output current of the converter. The prototype is implemented by using copper foil windings in the magnetic components and interconnections.

The two transformers with $n = 1/2$ are constructed using a stacked structure with four halves of E64/10/50 in 3F3 material. The input inductor is constructed with a Kool Mu core from Magnetics K6527E040. The converter prototype is shown in Fig. 19.

The converter is operated with a supercapacitor module from Maxwell $BM\,OD0130\,P056\,B03$ rated $56\,V$ and $130\,F$.

A controller composed of an integrator and a zero is designed and the loop crossover frequency is adjusted to 1 kHz for $V_B = 80\,V$ and $V_{SC} = 28\,V$ with an average inductor current of $I_L = 285\,A$. The duty cycle-to-output current transfer function has its maximum gain when the

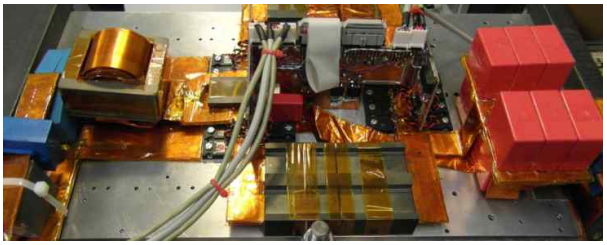

Fig. 19. Second PPIBC prototype.

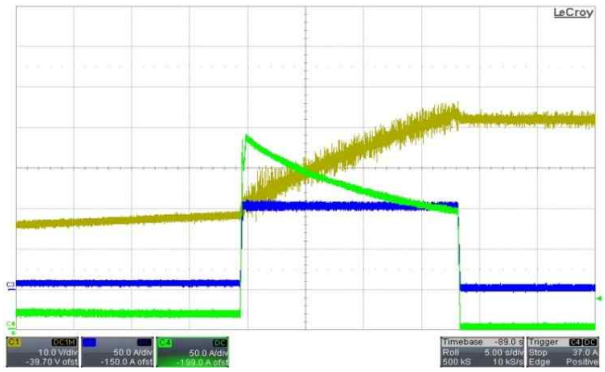

Fig. 20. Supercapacitor constant power charge event. Supercapacitor current (green, 50A/div). High side input current (blue, 50A/div) and supercapacitor voltage (light brown, 10V/div.)Time scale: 5s/div.

supercapacitor voltage is minimum. Therefore, by adjusting the controller for these operating conditions, stable operation of the converter can be guaranteed for the whole operating voltage of the supercapacitor. Fig. 20 shows a supercapacitor charge event with a constant input power level of 8 kW.

V. CONCLUSIONS

PPIBC is a high efficient isolated converter in low voltage high current applications. Bidirectional operation has been achieved by implementing synchronous rectification on the high voltage side. Accurate dynamic models have been derived and two different control strategies have been proposed for operation with supercapacitors.

Converter safe startup with batteries and supercapacitors regarding component stress is a non-trivial situation. The implemented DSP startup procedure proves that a soft start control of the current can be obtained and operation of the converter without any additional startup circuitry can be achieved.

The converter dynamic model has been shown to be the same independent of the power flow direction. The duty cycle-to-inductor plant transfer function is independent of the converter operating mode; therefore, a unified controller can be used for this control method. However, the duty cycle-to-output current transfer function dynamics present different behavior depending on the current flow direction due to the presence of a right half plane zero in boost operation mode. This situation forces the designer to implement two different controllers in order to maximize the dynamic performance of the control loops for each operation mode.

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Wide Operating Voltage Range Fuel Cell Battery Charger

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Wide Operating Voltage Range Fuel Cell Battery Charger

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***Abstract*—DC-DC converters for fuel cell applications require wide voltage range operation due to the unique fuel cell characteristic curve. Primary parallel isolated boost converter (PPIBC) is a boost derived topology for low voltage high current applications reaching an efficiency figure up to 98.2 %. This paper proposes a new operation mode for extending the input and output voltage range in PPIBC. The proposed solution does not modify PPIBC power stage; the converter gain is modified by short-circuiting one of the parallel connected primary windings in the topology. The change in operation mode divides by two the converter input-to-output voltage gain. This allows covering the conditions when the fuel cell stack operates in the activation region (maximum output voltage) and increases the degrees of freedom for converter optimization. The transition between operating modes is studied because represents a change in the converter steady-state conditions. A solution is proposed based on pre-calculation of the duty cycle prior to the transition.**

***Index Terms*—Isolated boost, fuel cell, battery, extended voltage range.**

I. INTRODUCTION

Due to the need for alternative energy resources, efficient power processing through power electronics circuits has been a popular academic field for the past decade. Fuel cells are one of the solutions widely adopted in uninterruptible power supplies (UPS), backup systems and electric vehicles. Fuel cells provide a clean and consistent source of energy by converting chemical energy into electrical energy. Power electronics interfacing fuel cell stacks and the rest of the power system should be designed considering some important electrical features of the fuel cell system, such as V-I characteristic curve. Among various converter topologies proposed and used in the literature, primary parallel isolated boost converter (PPIBC), derived from the conventional isolated boost converter, is a good candidate for such applications due to its simplicity and ability to handle high currents [1], [2]. However, boost type dc-dc converters have intrinsic start-up problems and limited input/output voltage range operation. Overcoming this limitation requires modification of the input inductor and employing additional circuitry [3]. In this paper an alternative solution with an extended voltage operation range is proposed based on modifying the operating mode of PPIBC. PPIBC schematic and steady-state operating waveforms under normal operating conditions are presented in Fig. 1 and Fig. 2.

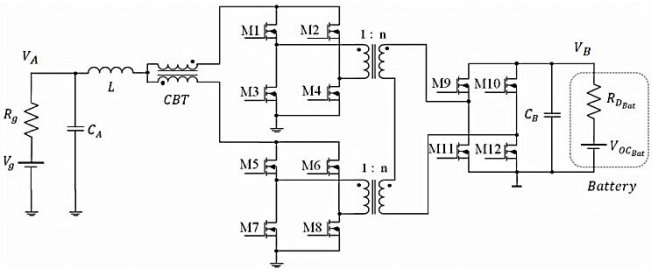

Fig. 1. Primary parallel isolated boost converter schematic.

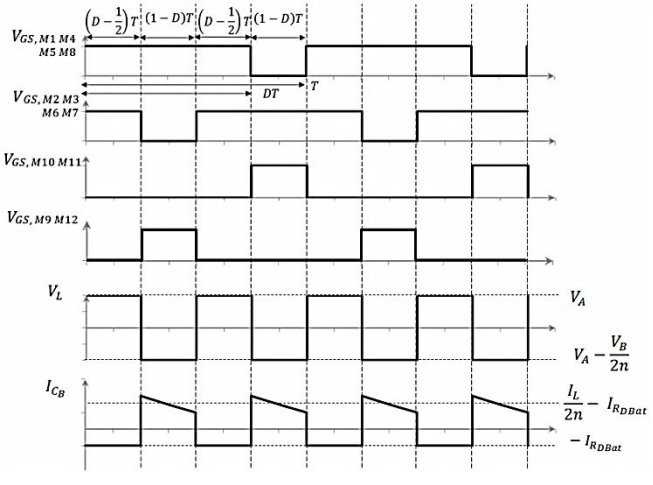

Fig. 2. Primary parallel isolated boost converter steady-state waveforms.

This topology increases the efficiency by splitting the primary current through two parallel primary stages. This approach results in reduced ac current loops, which helps reducing the power stage layout stray inductances. In addition, the secondary windings of the two transformers are connected in series, which reduces the number of turns on the secondary side for individual transformers allowing an

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easier magnetic component design. The primary switches in each parallel stage are driven with identical gate signals. Moreover, the two stages share the input inductor as well as the input and output filters, which makes this topology a simple solution. Due to the transformer series connection on the secondary side the two currents flowing through the two primary stages are forced to be equal during the inductor discharge state. In order to balance the current between the primary stages during the inductor charging subinterval, a current balancing transformer (CBT) [4] is inserted. This component is implemented as two inversely coupled inductors that present high impedance in case of current. imbalance, keeping the current equal in each parallel stage.

In this work, PPIBC acts as a battery charging unit in a fuel cell powered electric drive train in a low speed vehicle, as shown in Fig. 3. The V-I characteristic curve of a fuel cell is a nonlinear function [5], where three different regions can be distinguished as shown in Fig. 4. Moreover, as presented in the Shepherd model [6], the battery terminal voltage strongly depends on the charging current. Due to the battery terminal voltage dependence and the voltage rise in the activation region of the fuel cell (see Fig. 4), the converter needs to be designed for a wide operating input and output voltage range. When an acceleration event occurs, the inverter current demand will reduce the battery terminal voltage; if the fuel cell stack is operating in the activation region during this event, the converter will have to present minimum input to output voltage gain.

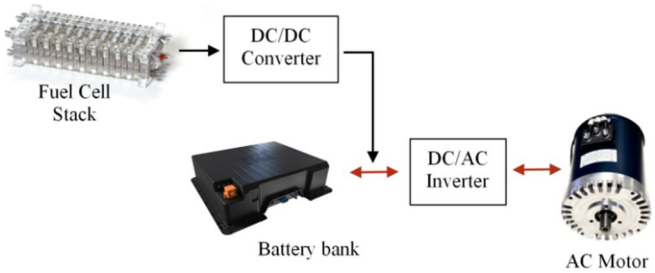

Fig. 3. Power drive train block diagram.

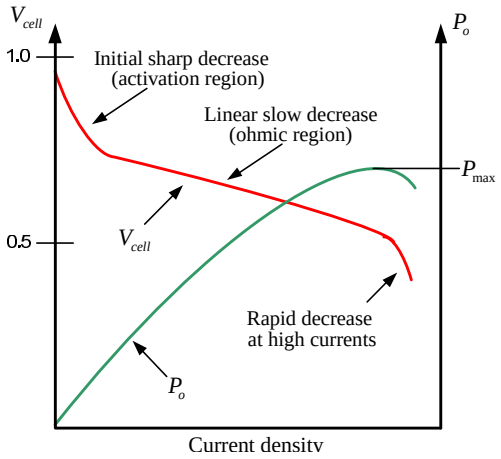

Fig. 4. Fuel cell characteristic V-I curve.

Therefore, in this application the transformer turns ratio has to be selected for the converter to operate with minimum duty cycle under these operating conditions. However, this solution will increase the converter voltage and current stresses negatively affecting the efficiency. Instead, this paper proposes a change in the converter operation mode, which increases the degrees of freedom in the design for the converter optimization.

II. Extended Operating Voltage Range

One of the disadvantages of isolated boost type dc-dc converters is the 50 % theoretical minimum duty cycle for each primary side switch, which corresponds to a “no boosting” operating point. Further decreasing the duty cycle is not possible since this will result in a practical “open circuit” situation for the input inductor. This lower limit for the switch duty cycle also puts a lower limit for the output voltage or an upper limit for the input voltage. The state of the art solution for extended voltage range in isolated boost converters has been presented in the literature [3], [7]. The solution in [3] proposes an auxiliary winding in the input inductor that will provide flyback operation to the converter, extending the operating voltage range and solving the intrinsic start-up problems in boost derived topologies. However, this is not an efficient solution in high power applications and makes the manufacturing process of the input inductor more complicated since extensive interleaving techniques will have to be adopted to increase the coupling coefficient of the flyback winding.

This work presents an efficient solution for extending the voltage range of PPIBC by implementing a new operation mode where the two upper side MOSFETs in one of the parallel stages are shut down while the lower side switches are kept in conduction mode. This new operation mode effectively reduces the equivalent converter conversion ratio by short-circuiting the primary winding in one of the primary stages, which deactivates the corresponding transformer.

As in the auxiliary flyback winding configuration, the main drawback of the proposed solution is the increased voltage stress on the primary switches during the extended operation mode. As shown in (3) the output voltage is no more divided in the series secondary windings of the two transformers. This situation will increase the requirement for the primary switch breakdown voltage, consequently increasing the device on resistance, which affects the converter efficiency. However, if the extended operation mode is only used to cover the operating conditions with minimum output voltage, the primary MOSFETs breakdown voltage requirement will not be affected.

$$V_{DS_{PPIBC}} = V_B / (2n), \quad (1)$$

$$V_{DS_{Flyback}} = V_A + V_B / (2n), \quad (2)$$

$$V_{DS_{PPIBC\_Extended}} = V_B / n. \quad (3)$$

This is an attractive solution in applications with variable output voltage, where the extended mode will be operated only under minimum output voltage.

Figure 5 shows the current path at the inductor discharge subinterval during extended operation mode of the PPIBC. As it can be observed from Fig. 5, the primary winding of the lower transformer is effectively shorted by the two low side switches, M7 and M8. The converter steady-state

waveforms are presented in Fig. 6. Figure 7 shows the converter voltage gain during extended voltage range operation; since only one transformer is active, effective voltage conversion ratio of the converter is halved as shown in (4).

$$M\left(D\right)=V_B/V_A=n/\left[2\left(1-D\right)\right]. \quad (4)$$

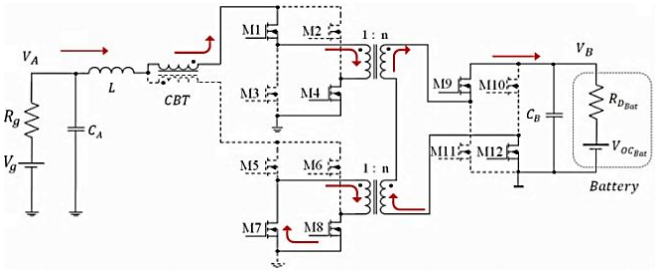

Fig. 5. PPIBC inductor discharge during extended voltage range mode.

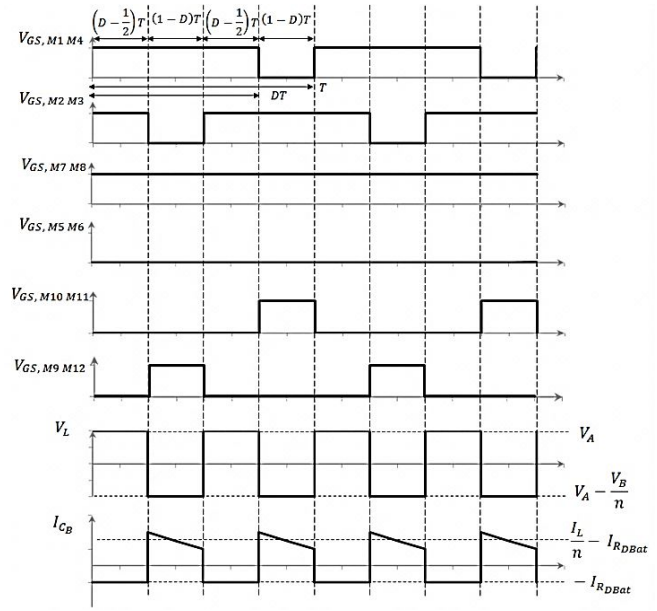

Fig. 6. PPIBC steady-state waveforms during extended voltage range operation.

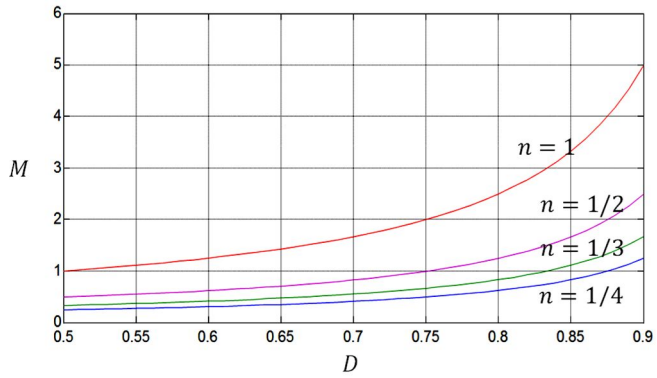

Fig. 7. Converter input to output voltage gain during extended operation mode for different transformer turns ratio.

III. SIMULATION OF PPIBC WITH EXTENDED VOLTAGE RANGE OPERATION

The proposed solution is analysed by performing several LTspice simulations with the operating conditions shown in Table I. The transition of the converter between normal and extended operation mode needs to be investigated because the output current of the fuel cell should be stable during this event. If the operation of the converter has to be interrupted to switch from one mode to the other, a dummy load would have to be used in order to limit the output voltage of the fuel cell during the transition, and this would increase the complexity of the system.

TABLE I. PARAMETERS OF THE CONVERTER.

Source voltage	30 V
Battery terminal voltage	24 V
Transformer turn ratio	3: 1
Inductor	13.5 µH
Capacitor A	40 µF
Capacitor B	120 µF
Switching frequency	50 kHz
Source output resistance	10 mΩ
Battery dynamic resistance	60 mΩ

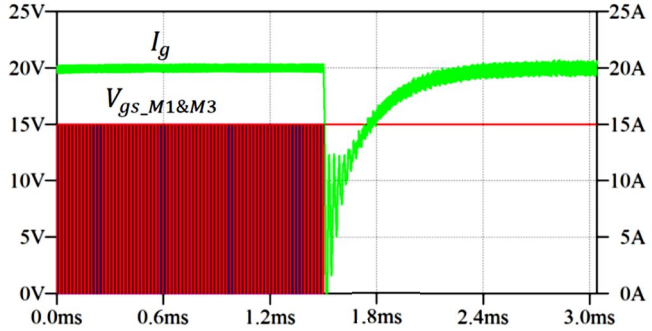

Fig. 8. Simulated transition from normal operation mode to extended operation mode. Converter input current I_g (green), M1 and M3 gate signal (red and blue).

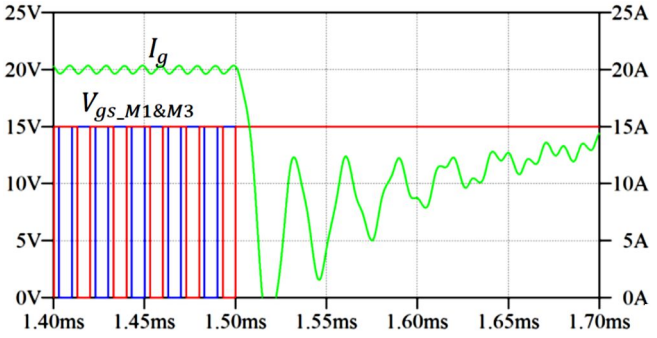

Fig. 9. Detailed enlarged area of the transition. Converter input current I_g (green), M1 and M3 gate signal (red and blue).

Figure 8 and Fig. 9 present a simulation result where the inductor current level is fixed at $20A$ during closed loop operation of the converter. It can be observed that during the transition the current deviates from the reference value until the loop is able to compensate the error. The deviation in the current during the transition is caused by the change in the converter steady-state conditions and the sensitivity of the inductor current to duty cycle perturbations, as presented in [8]. This will increase the components current stress, which will reduce the converter reliability.

IV. TRANSITION WITH PRE-CALCULATED STEADY-STATE DUTY CYCLE

The current stress during the transition time can be

reduced if a steady-state duty cycle pre-calculation is performed based on an accurately derived model of the converter. In battery loading applications, as presented in [8]–[9], the duty cycle-to-inductor current transfer function is heavily affected by the converter parasitic resistances due to the low value of the battery dynamic resistance. Circuit models taking into account parasitic resistances for both inductor charge (Fig. 10) and discharge (Fig. 11) states during extended operation mode are derived. The simplified models, shown in Fig. 12 and Fig. 13, are obtained by reflecting the secondary side impedances to the primary side and combining the two parallel full-bridge transformers to a single structure with an effective transformer ratio N_e.

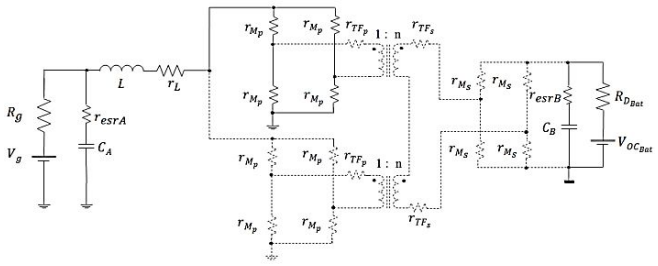

Fig. 10. PPIBC extended voltage range operation during the inductor charging subinterval.

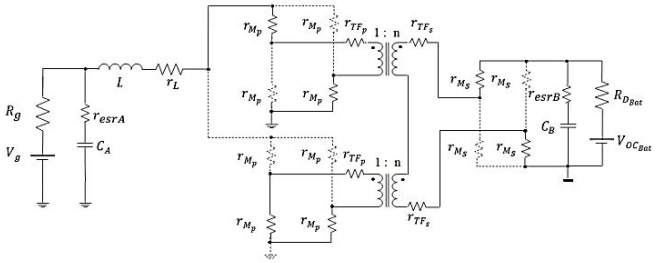

Fig. 11. PPIBC extended voltage range operation during the inductor discharging subinterval.

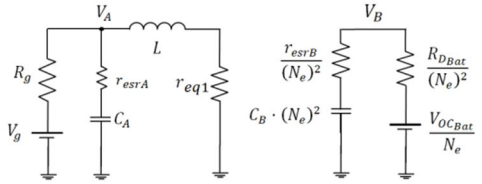

Fig. 12. PPIBC simplified equivalent circuit during the inductor charge.

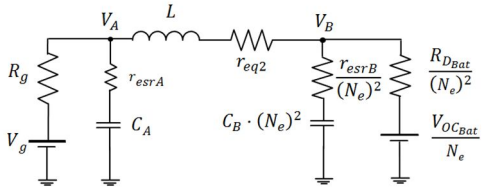

Fig. 13. PPIBC simplified equivalent circuit during the inductor discharge.

State-space equations are derived based on the two operating states of the converter [8]. The state matrixes are calculated for the inductor charging and discharging subintervals as shown in (16) and (17). The input matrix corresponding to the inductor charging subinterval is shown in (5), and the input matrix corresponding to the discharging subinterval is calculated as shown in (6):

$$B_1 = \begin{pmatrix} r_{esr_A} / \left[L\left(R_g + r_{esr_A}\right)\right] & 0 \\ 1/\left[C_A\left(R_g + r_{esr_A}\right)\right] & 0 \\ 0 & 1/\left[2C_B N_e\left(R_{D_{Bat}} + r_{esrB}\right)\right] \end{pmatrix}, \quad (5)$$

$$B_2 = \begin{pmatrix} r_{esr_A} / \left[L\left(R_g + r_{esr_A}\right)\right] & -r_{esr_A} / \left[2N_e L\left(R_{D_{Bat}} + r_{esrB}\right)\right] \\ 1/\left[C_A\left(R_g + r_{esr_A}\right)\right] & 0 \\ 0 & 1/\left[2C_B N_e\left(R_{D_{Bat}} + r_{esrB}\right)\right] \end{pmatrix}. \quad (6)$$

Equivalent transformation ratio N_e and equivalent resistances r_{eq1} and r_{eq2} are defined as shown in (7)–(9) for normal operating mode. These can be calculated in the same way for extended operating mode as shown in (10)–(12):

$$N_e = 2n, \quad (7)$$

$$r_{eq1} = r_L + r_{M\,P} / 2, \quad (8)$$

$$r_{eq2} = r_L + r_{M\,P} + r_P / 2 + \\ +2r_S / (2n)^2 + 2r_{M\,S} / (2n)^2, \quad (9)$$

$$N_e = n, \quad (10)$$

$$r_{eq1} = r_L + r_{M\,P}, \quad (11)$$

$$r_{eq2} = r_L + 4r_{M\,P} + 2r_P + \\ +2r_S / n^2 + 2r_{M\,S} / n^2. \quad (12)$$

Based on the conduction states shown in Fig.10 and Fig. 11, a new model can be obtained for normal and extended operating voltage mode. The state equation of the system is obtained as shown in (13)

$$d / dt \begin{pmatrix} i_L(t) \\ v_{C\,A}(t) \\ v_{C\,B}(t) \end{pmatrix} = A \cdot \begin{pmatrix} i_L(t) \\ v_{C\,A}(t) \\ v_{C\,B}(t) \end{pmatrix} + B \cdot \begin{pmatrix} V_g \\ V_{OC\,Bat} \end{pmatrix}. \quad (13)$$

The averaged value of the input and state matrixes is obtained by averaging (5), (6), (16) and (17) over the inductor period as shown in (14) and (15):

$$A = A_1 \cdot d + A_2 \cdot (1 - d), \quad (14)$$

$$B = B_1 \cdot d + B_2 \cdot (1 - d). \quad (15)$$

$$A_1 = \begin{pmatrix} -\frac{1}{L}\left(r_{eq1} + \frac{r_{esr_A} \cdot R_g}{R_G + r_{esr_A}} \right) & \frac{R_g}{L\left(R_g + r_{esr_A}\right)} & 0 \\ -\frac{R_g}{C_A\left(R_g + r_{esr_A}\right)} & -\frac{1}{C_A\left(R_g + r_{esr_{IN}}\right)} & 0 \\ 0 & 0 & -\frac{1}{C_B\left(R_{D_{Bat}} + r_{esr_B}\right)} \end{pmatrix}, \quad (16)$$

$$A_2 = \begin{pmatrix} -\frac{1}{L}\left(r_{eq2} + \frac{r_{esrB}\cdot R_{D_{Bat}}}{4N_e^2\left(R_{D_{Bat}} + r_{esrB}\right)} + \frac{r_{esr_A}\cdot R_g}{R_g + r_{esr_A}} \right) & \frac{R_g}{L\left(R_g + r_{esr_A}\right)} & -\frac{R_{D_{Bat}}}{L\left(R_{D_{Bat}} + r_{esrB}\right)} \\ -\frac{R_g}{C_A\cdot\left(R_g + r_{esr_A}\right)} & -\frac{1}{C_A\left(R_g + r_{esr_A}\right)} & 0 \\ \frac{R_{D_{Bat}}}{4\cdot C_B\cdot N_e^2\left(R_{D_{Bat}} + r_{esrB}\right)} & 0 & -\frac{1}{C_B\left(R_{D_{Bat}} + r_{esrB}\right)} \end{pmatrix}. \quad (17)$$

In order to reduce the current stress during the transition between normal and extended voltage range mode, the converter MOSFETs' duty cycle is computed prior to the transition by calculating the steady-state solution from (13) as shown in (18)

$$D = 2[1-(I_L\cdot\left(R_g + R_{D_{Bat}} / N_e{}^2 + r_{eq2}\right)+ +V_{OC\,Bat} / N_e - V_g) / (I_L\cdot(R_{D_{Bat}} / N_e{}^2 + +r_{eq2} - r_{eq1}) + V_{OC\,Bat} / N_e)]. \quad (18)$$

Equation (18) is simplfied by taking into account that the input and ouput capacitors do not affect the converter duty cycle-to-inductor current steady-state solution.

Nevertheless, a calculation based on this equation presents a very high computational demand because the battery dynamic resistance is strongly dependent on the battery state of charge (SOC). On the other hand, if the input and output voltages of the converter (V_A,V_B) are measured during operation, expression of (18) can be reduced to (19)

$$D = 2[1-\left(I_L\cdot r_{eq2} + V_B / N_e - V_A\right) / / \left(I_L\cdot\left(r_{eq2} - r_{eq1}\right) + V_B / N_e\right). \quad (19)$$

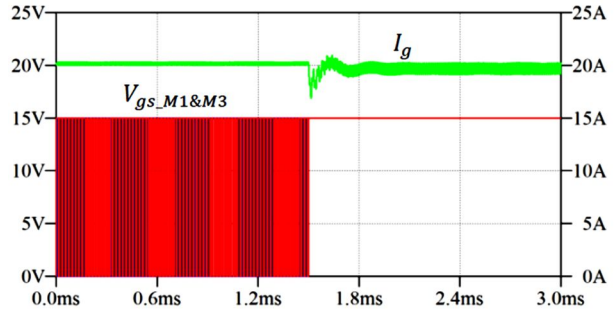

Fig. 14. Simulated transition between operating modes with pre-calculated steady-state duty cycle. Converter input current I_g (green), M1 and M3 gate signal (red and blue).

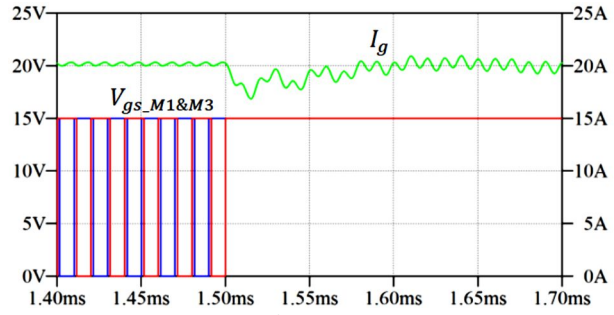

Fig. 15. Detailed enlarged area of the transition. Converter input current I_g (green), M1 and M3 gate signal (red and blue).

Figure 14 and Fig. 15 show an LTSpice simulation of a transition event where the controller has been set to produce the pre-calculated duty cycle before the transition event between normal and extended operating modes.

V. EXPERIMENTAL RESULTS

A digitally controlled PPIBC has been used to experimentally verify the operation of the converter in extended mode. Each of the converter magnetic components is implemented with four planar ELP64/10/50 parts in N87 material. The primary and secondary switches are 150V N-channel MOSFETs IRFP4568. The converter control board is based on a 32 bit fixed point digital signal processor (DSP) TMS320F28035. The gate signals in one of the paralleled primary stages have been modified by inserting some control logic circuitry to produce the desired waveforms under the extended operation mode. The implemented prototype and the gate drive circuitry are shown in Fig. 16 and Fig. 17 respectively. Figure 18 shows the prototype operating waveforms during normal operation mode.

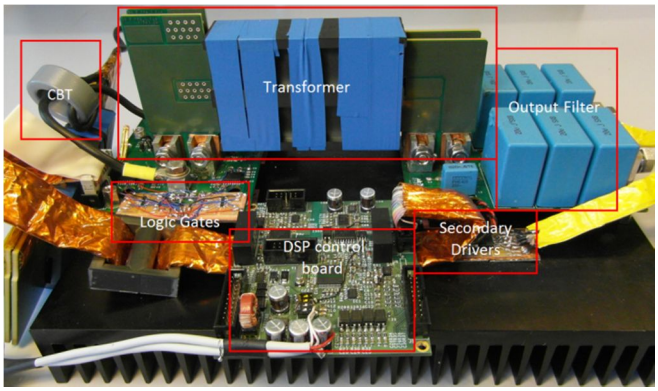

Fig. 16. PPIBC experimental prototype.

Figure 19 presents the converter operating waveforms during extended operating mode. The inductor current shows a change in the slope. During this mode, the magnetizing inductance of the current balancing transformer appears in series with the input inductor. However, the current balancing transformer saturates during this operation mode causing the change in the inductor current slope. The converter's efficiency in normal and extended operation modes can be observed in Fig. 20. The efficiency in the extended mode is measured at half the output voltage in normal mode. As it can be seen, the efficiency in extended operation mode decreases compared to the normal mode.

This is due to the higher current stress in the secondary side, the increased conduction losses in the primary side and

the increased transformer leakage inductance during the extended mode.

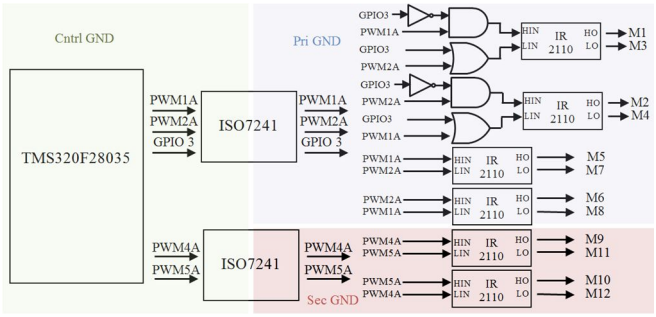

Fig. 17. Gate drive circuitry.

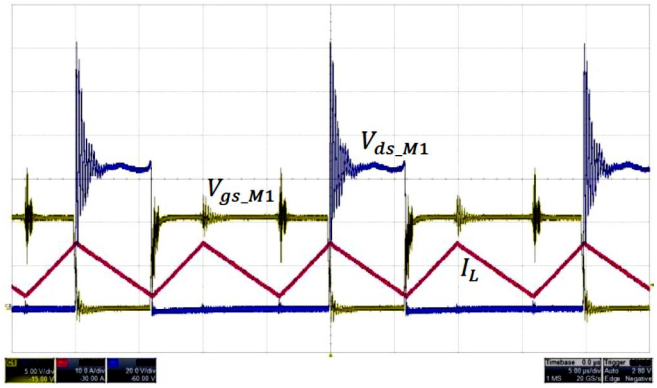

Fig. 18. Converter operating waveform during normal operation mode. M1 gate signal (brown, 5 V/div), M1 drain to source voltage signal (blue, 20 V/div) time scale 5 µs/div.

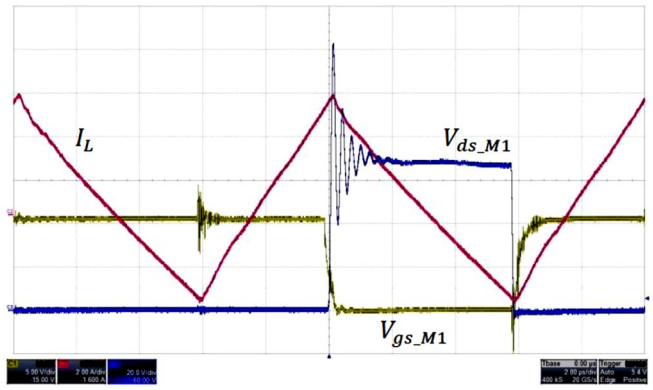

Fig. 19. Converter operating waveform during extended operation mode. M1 gate signal (brown, 5 V/div), M1 drain to source voltage signal (blue, 20 V/div) time scale 2 µs/div.

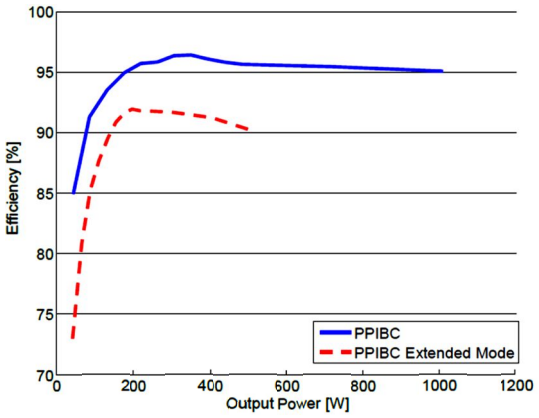

Fig. 20. Converter efficiency comparison between operating modes (blue, normal mode $V_{in} = 40\,V$ and $V_o = 45\,V$ and red $V_{in} = 40\,V$ and $V_o = 22.5\,V$).

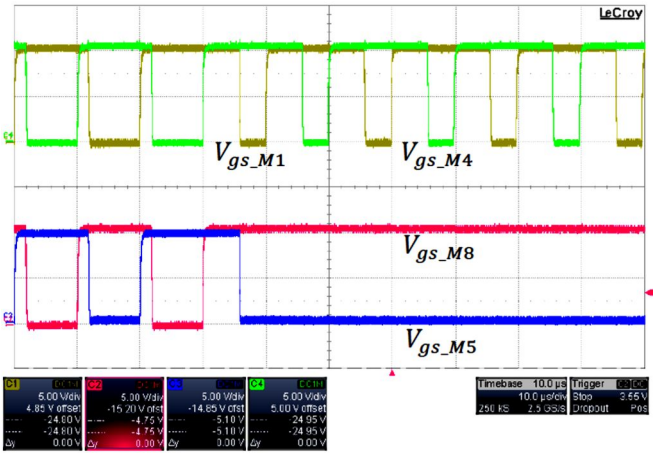

Fig. 21. Gate waveforms during normal to extended operating mode transition (b). M1 and M4 gate signals (brown and green, 5 V/div), M5 and M8 gate signals (blue and red, 5 V/div) time scale 100 µs/div.

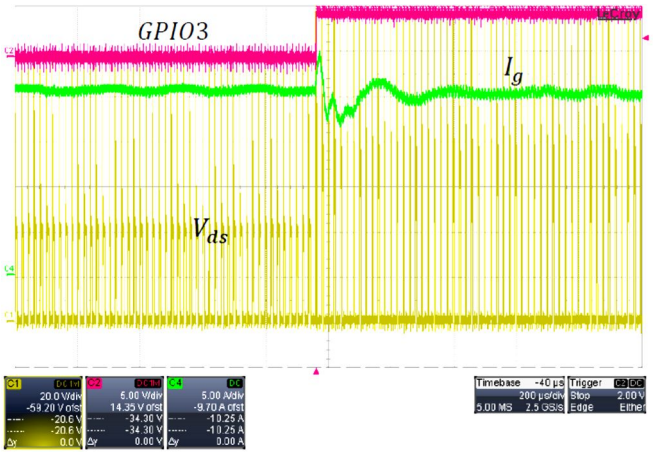

Fig. 22. Transition between operating modes with pre-calculated steady-state duty cycle. Time scale: 200 µs/div. Source output current I_g (green, 5 A/div), primary MOSFET drain to source voltage (brown, 20 V/div) and short circuit control signal GPIO3 (red, 5 V/div).

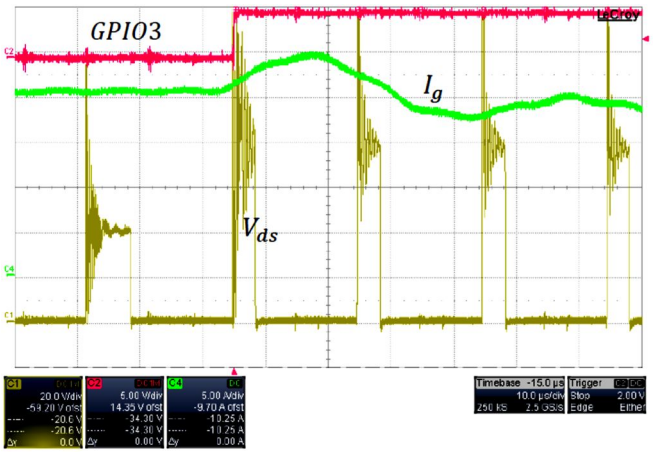

Fig. 23. Detailed zoomed waveforms of the transition Time scale:10 µs/div). Source output current I_g (green, 5 A/div), primary MOSFET drain to source voltage (brown, 20 V/div) and short circuit control signal GPIO3 (red, 5 V/div).

Figure 21–Fig. 23 show a transition event from normal to extended operating mode with pre-calculated duty cycle during converter closed loop operation for an inductor current level equal to 20 A. The change in duty cycle and voltage stress can be observed in one of the primary MOSFETs drain to source voltage waveform. It can be noticed that during extended operation mode, the voltage

ringing at the MOSFET off state increases with respect to the normal operation mode due to the effect of the leakage inductance of the short circuited transformer.

VI. CONCLUSIONS

In applications requiring wide operating voltage ranges, extreme duty cycles and extreme turn ratios for transformers have to be selected for covering the converter specifications, which will affect converter efficiency. Therefore, optimizing converter design for the most probable operating conditions and still covering all the possible operating points is desired. In order to do this, a new method for extending the operating voltage range has been proposed for PPIBC. The effective converter voltage conversion ratio is changed by deactivating one of the transformers through short-circuiting its primary windings. This new operation mode has been tested in a series of simulations and experiments where it has been observed that the transition between normal and extended operating modes is a disturbance to the converter due to the change in steady-state operating conditions. However, a smooth transition can be obtained if the steady-state duty cycle is pre-calculated based on an accurate model of the converter. This is an alternative solution to the auxiliary flyback winding in PPIBC.

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